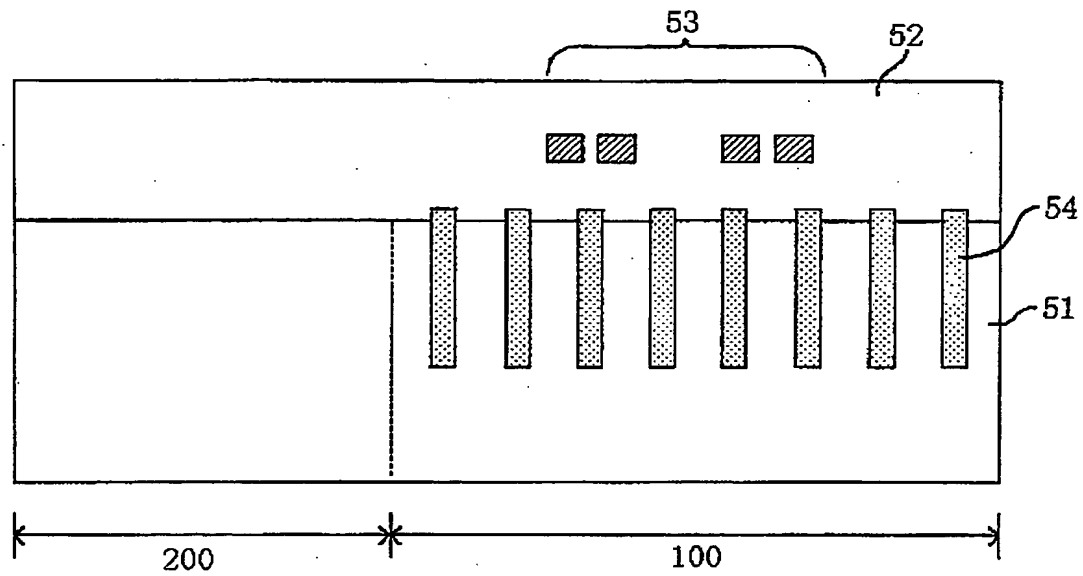


Fig. 1



51 SEMICONDUCTOR SUBSTRATE  
52 LAYERED FILM  
53 INDUCTOR

54 LOW-PERMITTIVITY FILLING MEMBER  
100 RF CIRCUIT AREA  
200 DIGITAL CIRCUIT AREA

Fig. 2

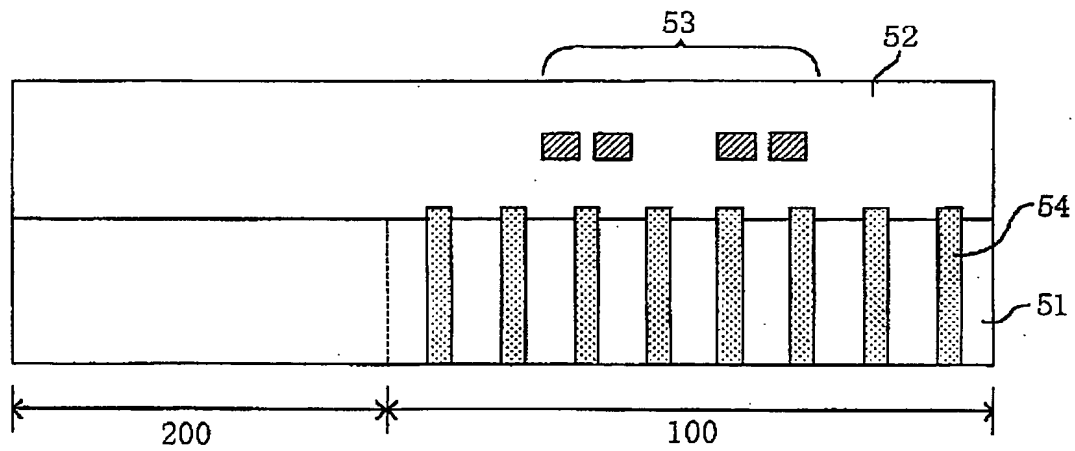


Fig. 3

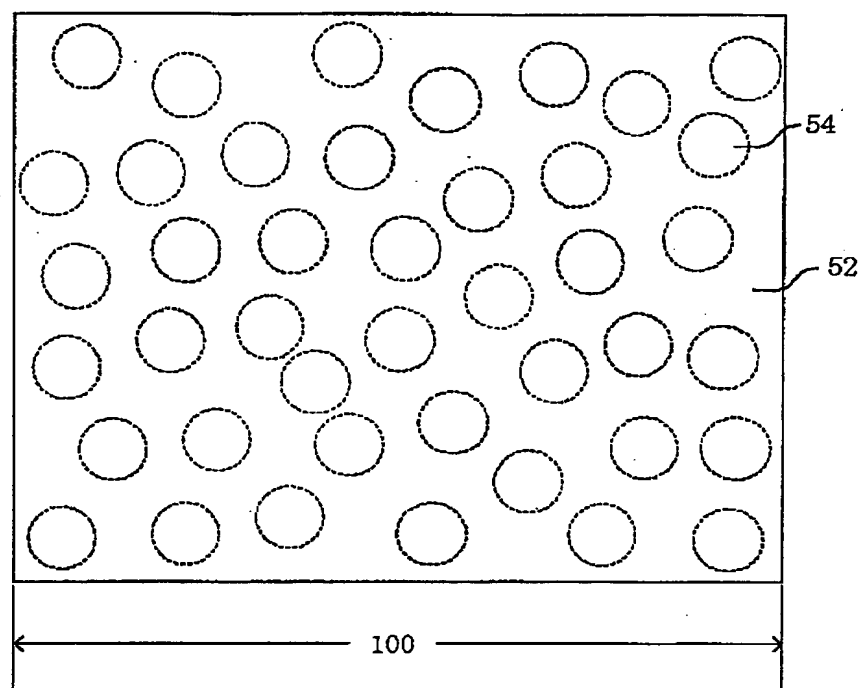


Fig. 4

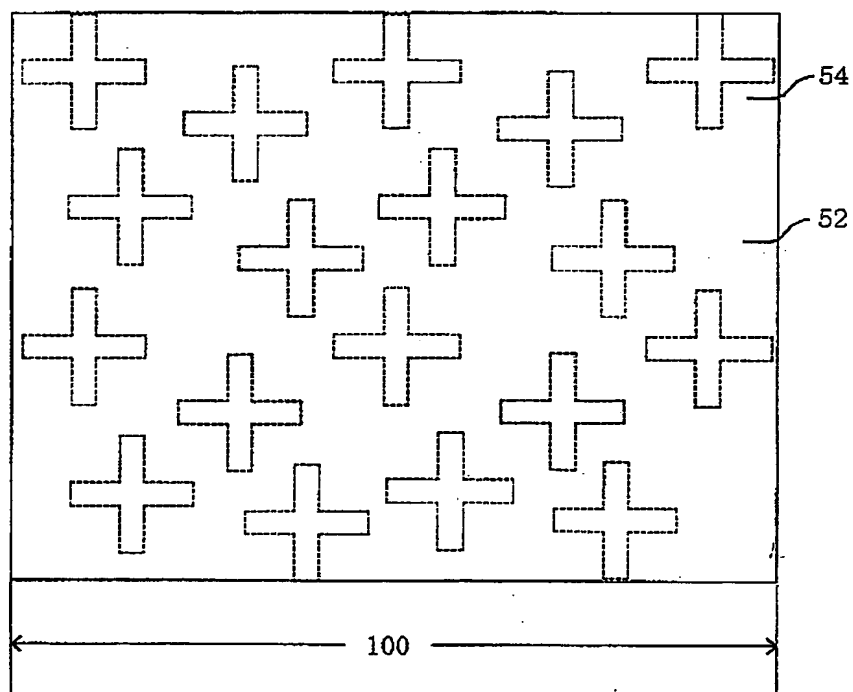
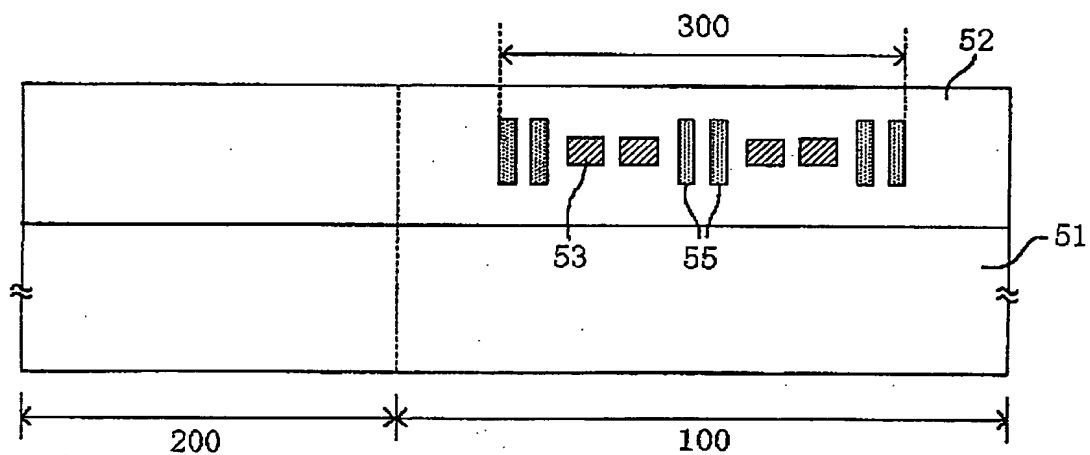
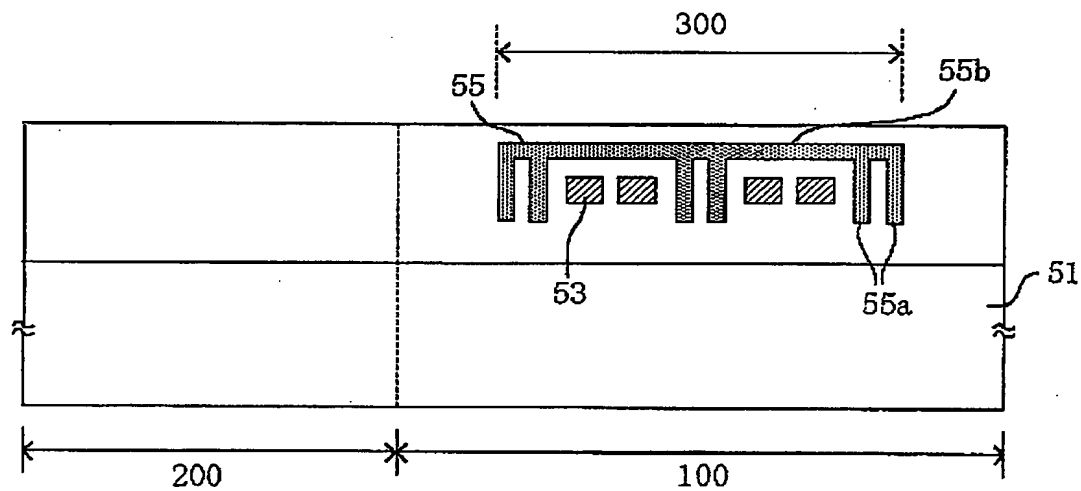


Fig. 5



55 HIGH PERMEABILITY FILLING MEMBER  
300 HIGH-PERMEABILITY AREA

Fig. 6



55A ROD MEMBER  
55B PLANE MEMBER

Fig. 7

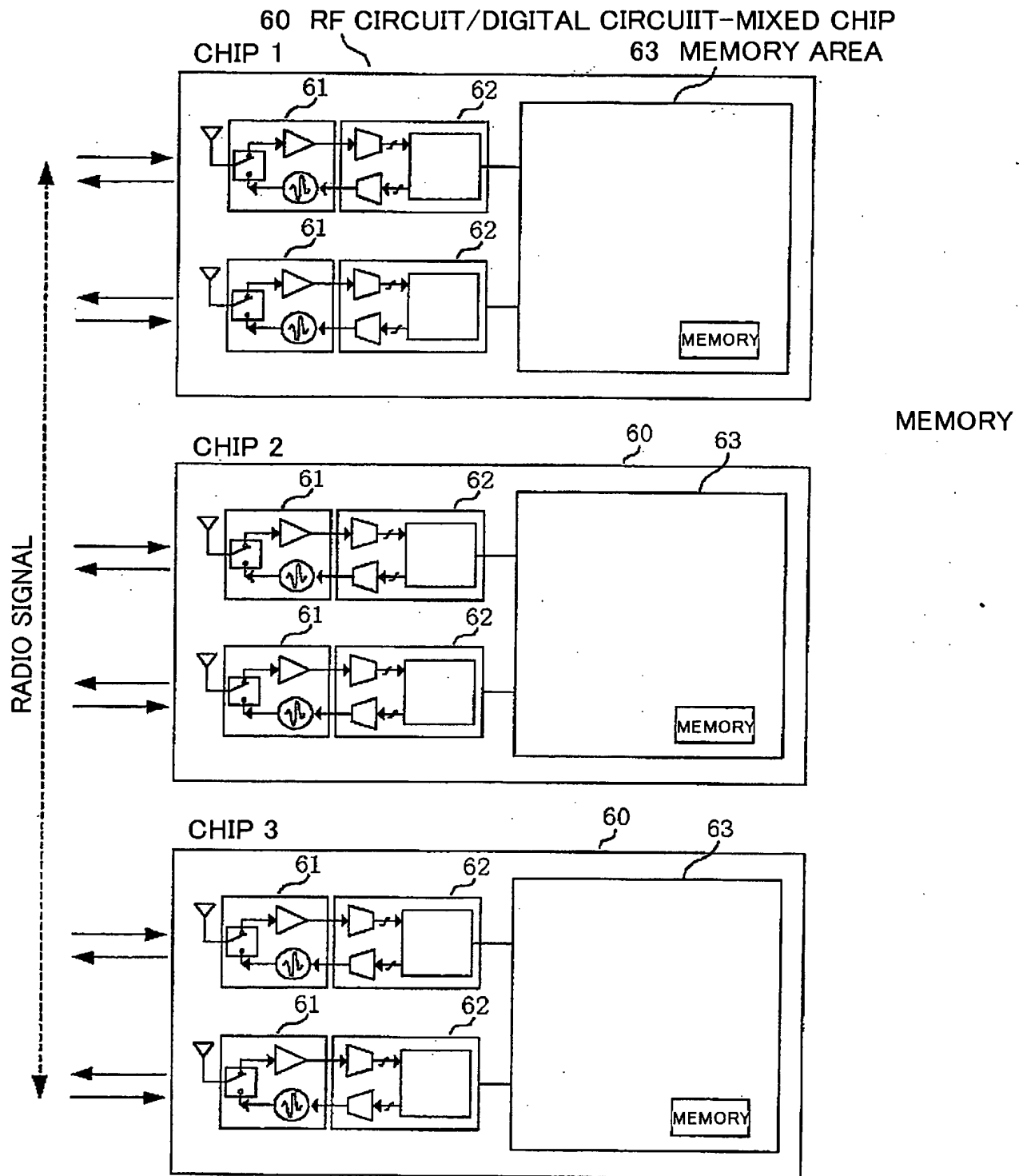


Fig. 8

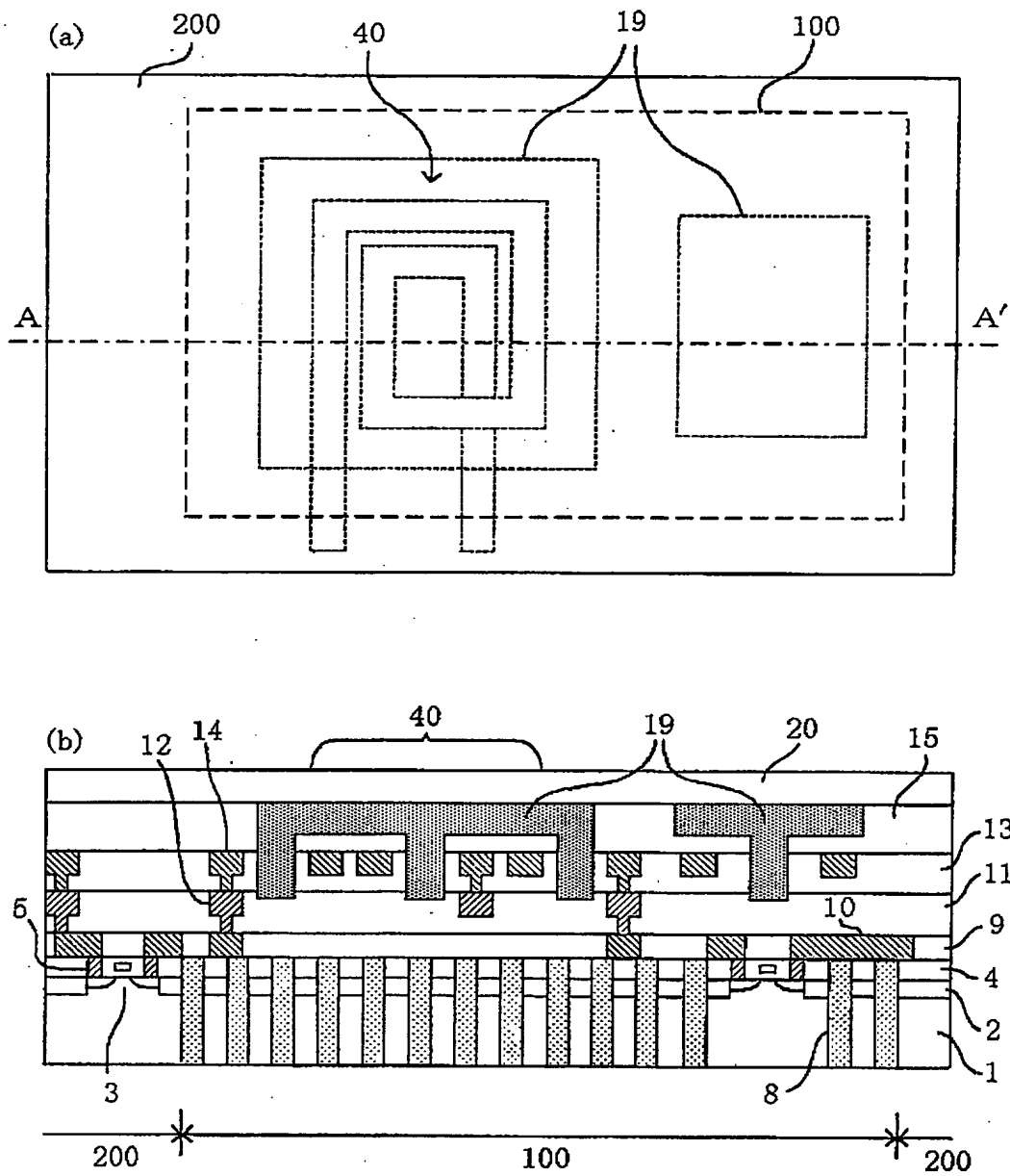


Fig. 9

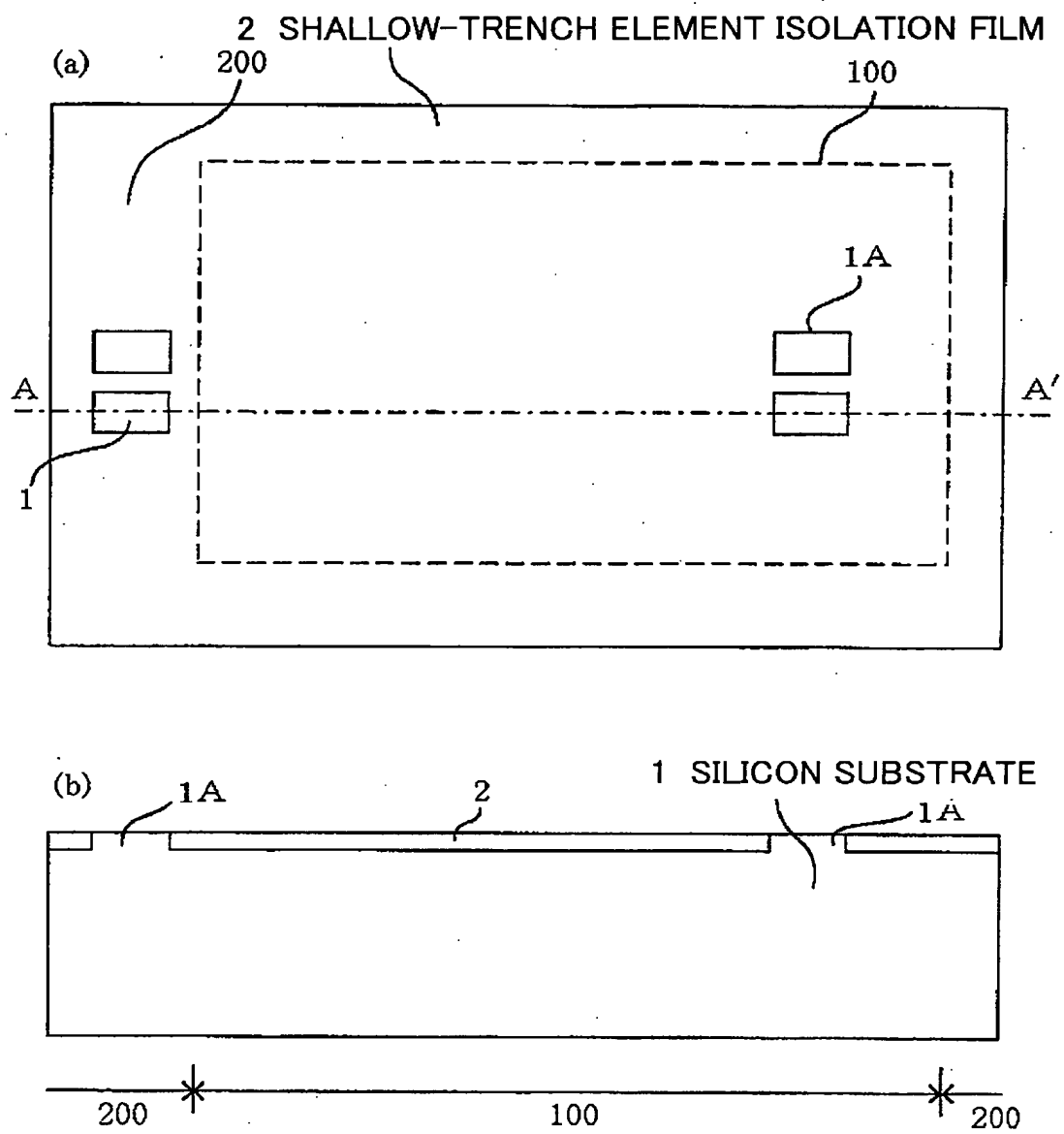


Fig. 10

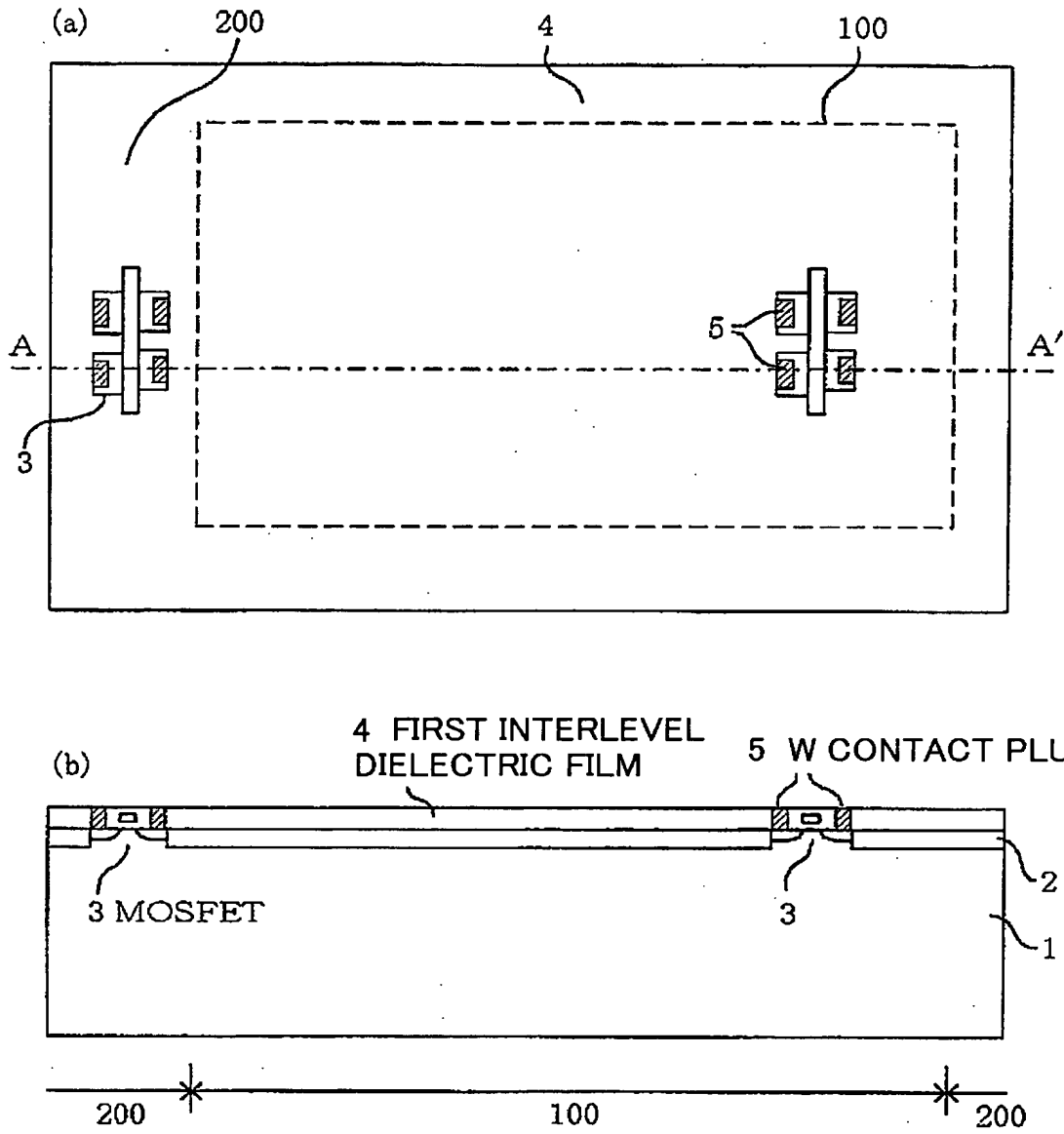


Fig. 11

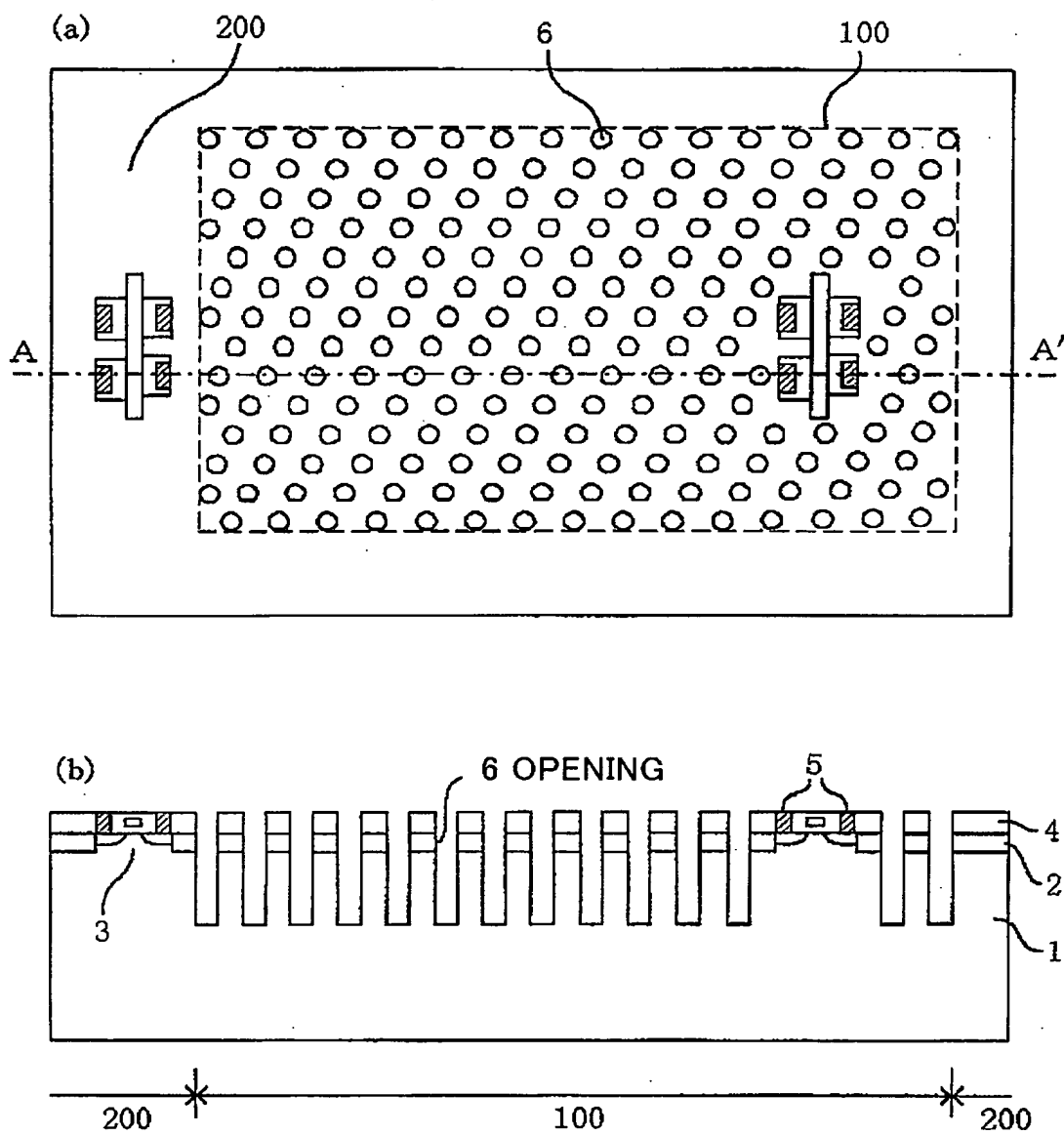




Fig. 12

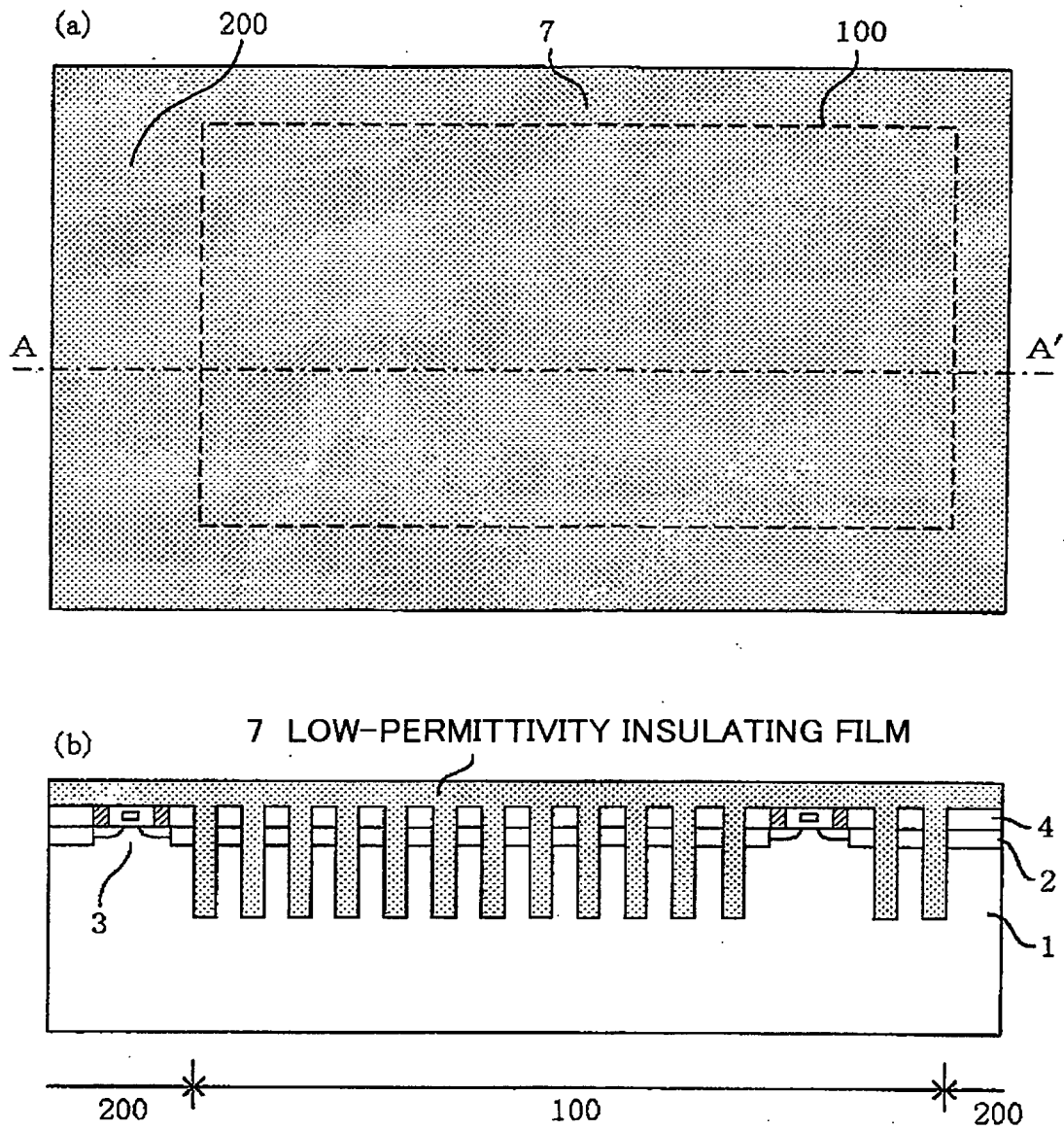


Fig. 13

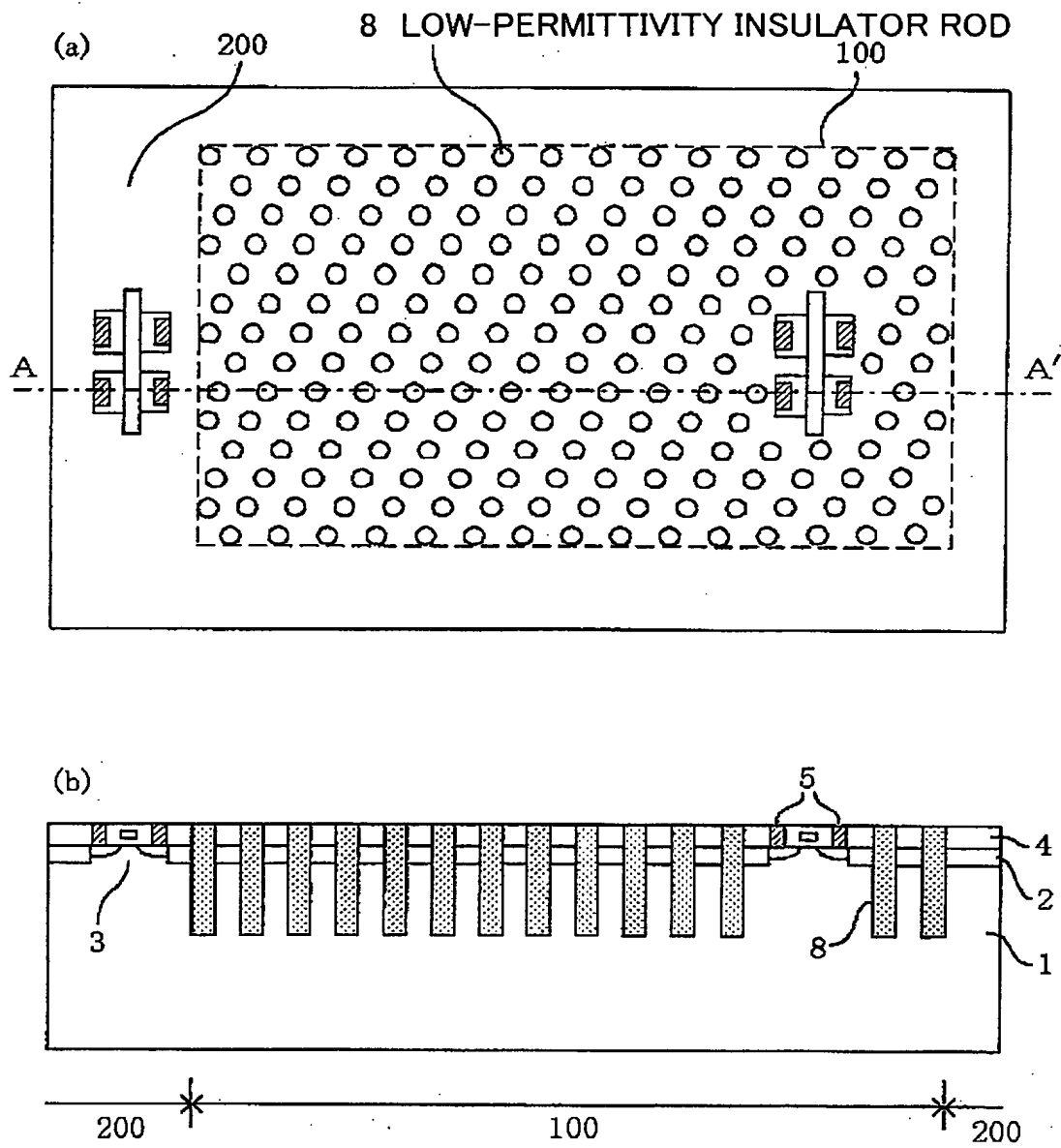


Fig. 14

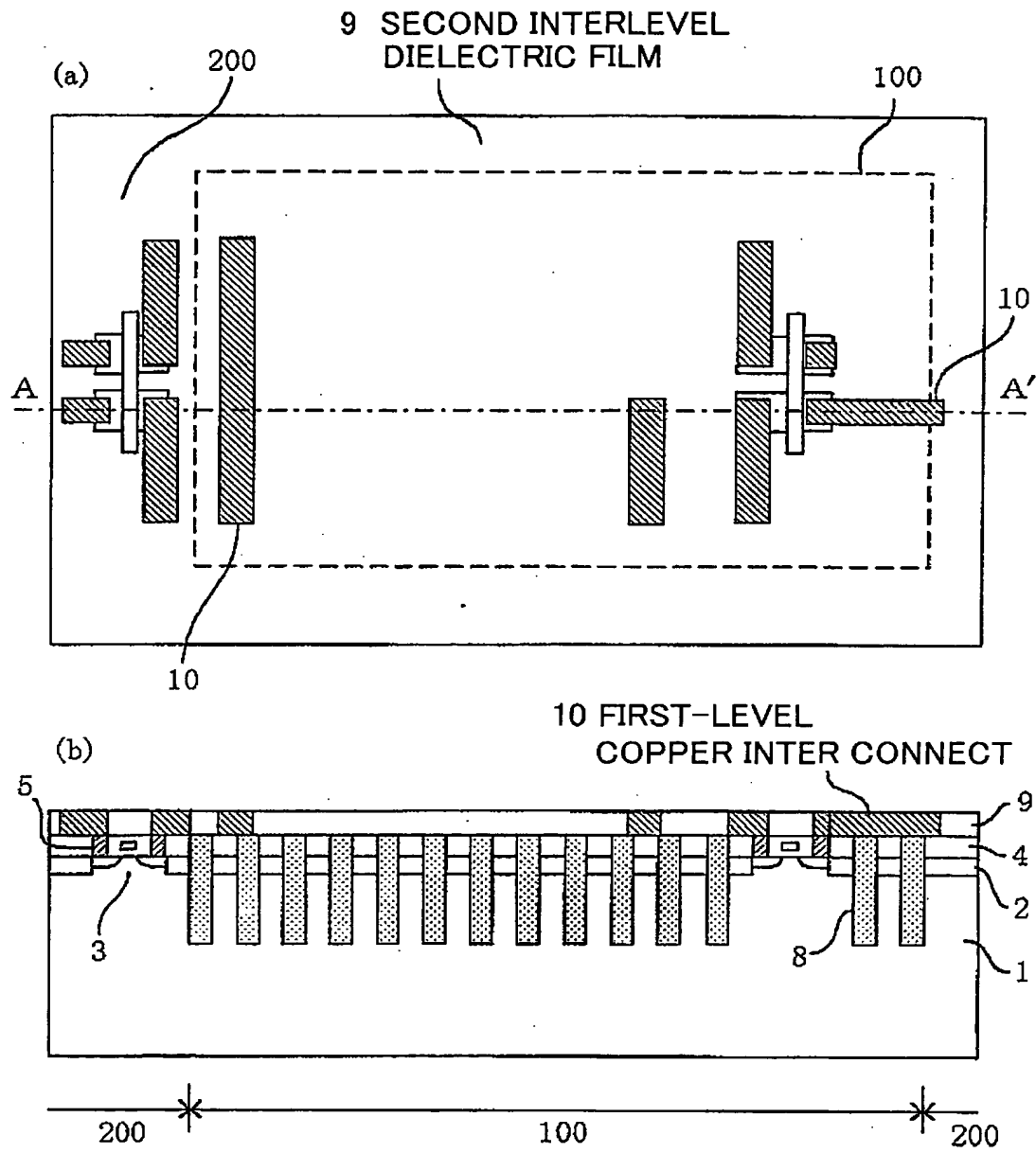
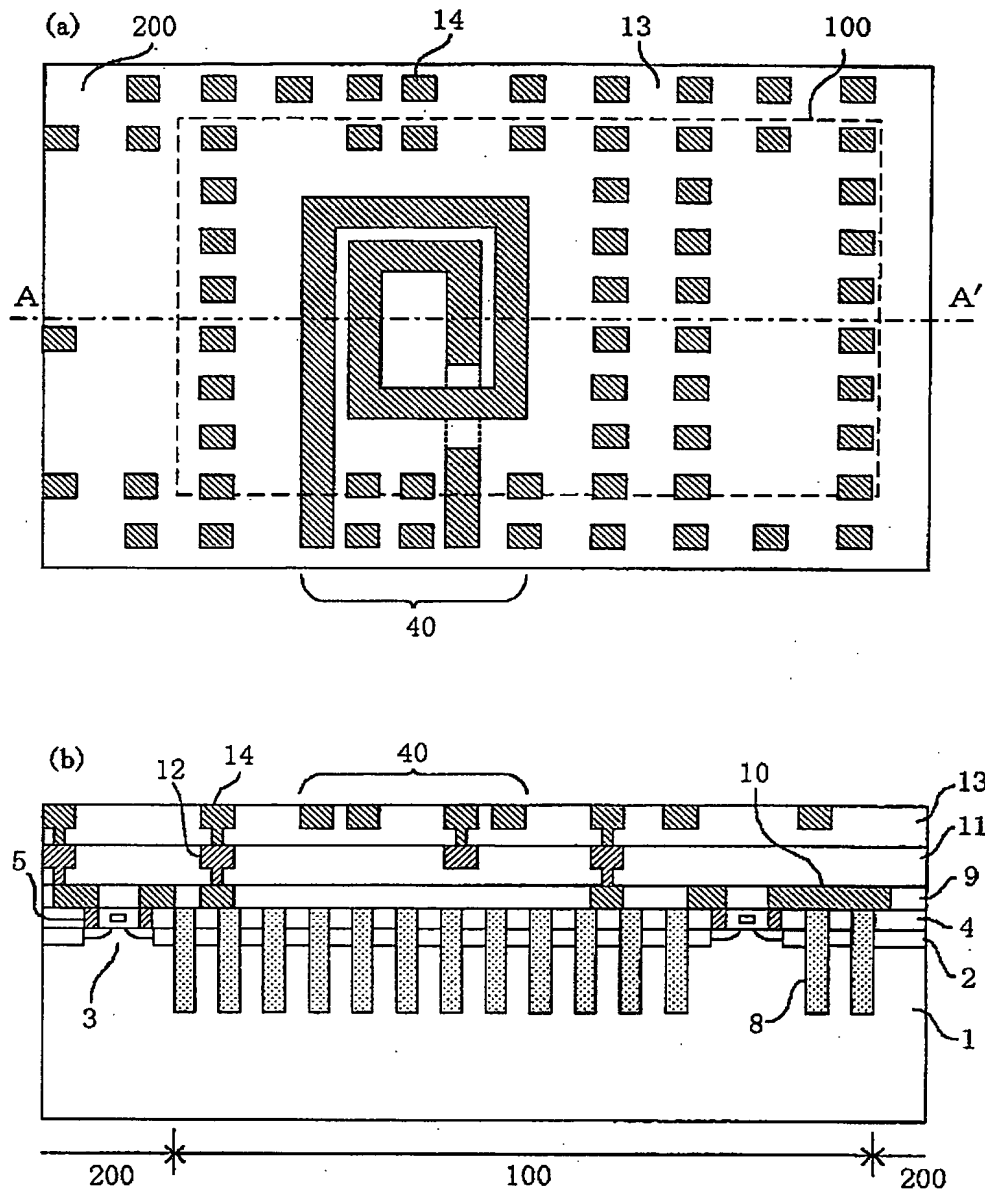
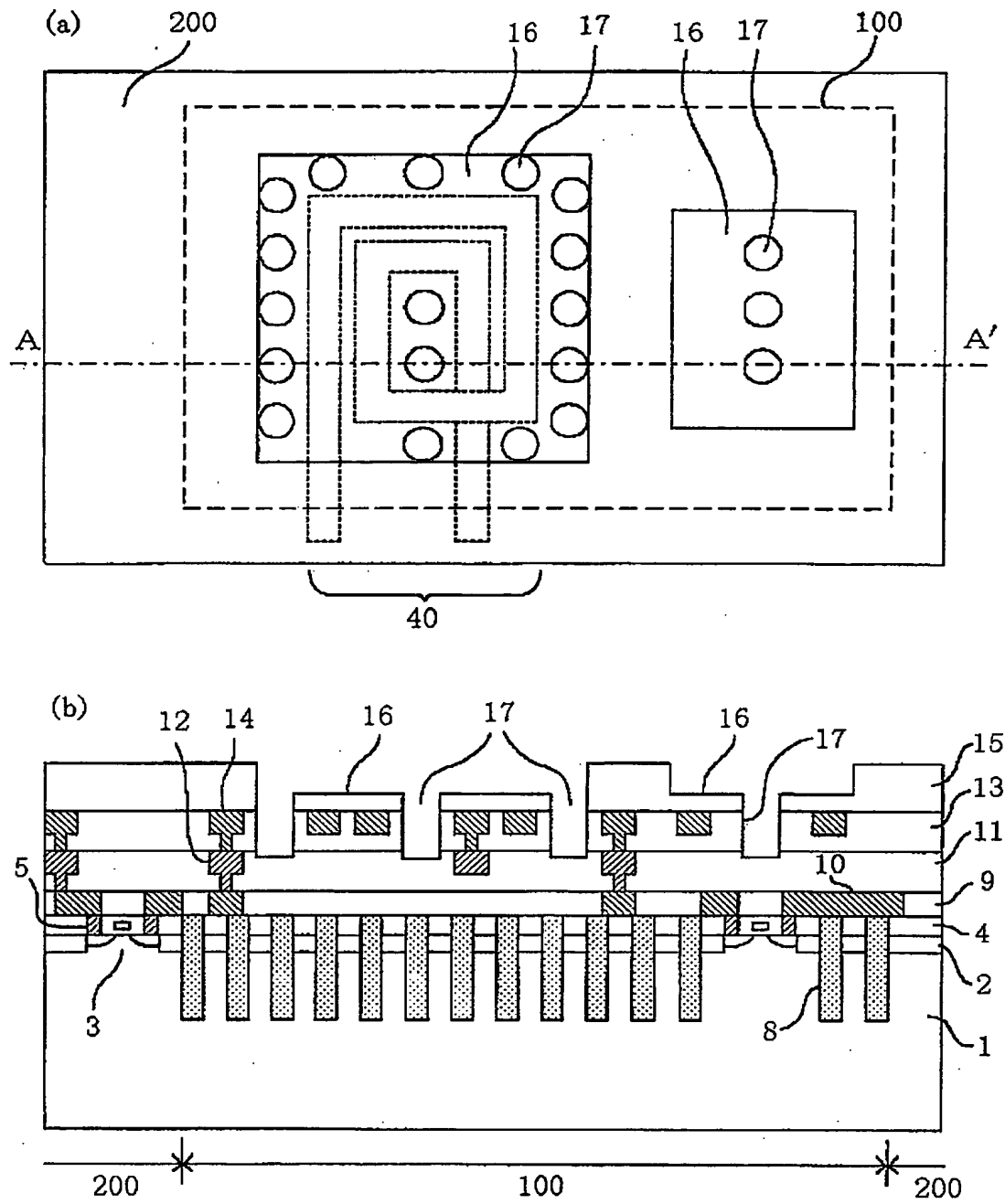


Fig. 15



- 11 THIRD INTERLEVEL DIELECTRIC FILM
- 12 SECOND INTERLEVEL DIELECTRIC FILM
- 13 FOURTH INTERLEVEL DIELECTRIC FILM
- 14 THIRD-LEVEL COPPER INTERCONNECT
- 40 INDUCTOR

Fig. 16



15 FIFTH INTERLEVEL DIELECTRIC FILM  
 16 DEPRESSION  
 17 OPENING

Fig. 17

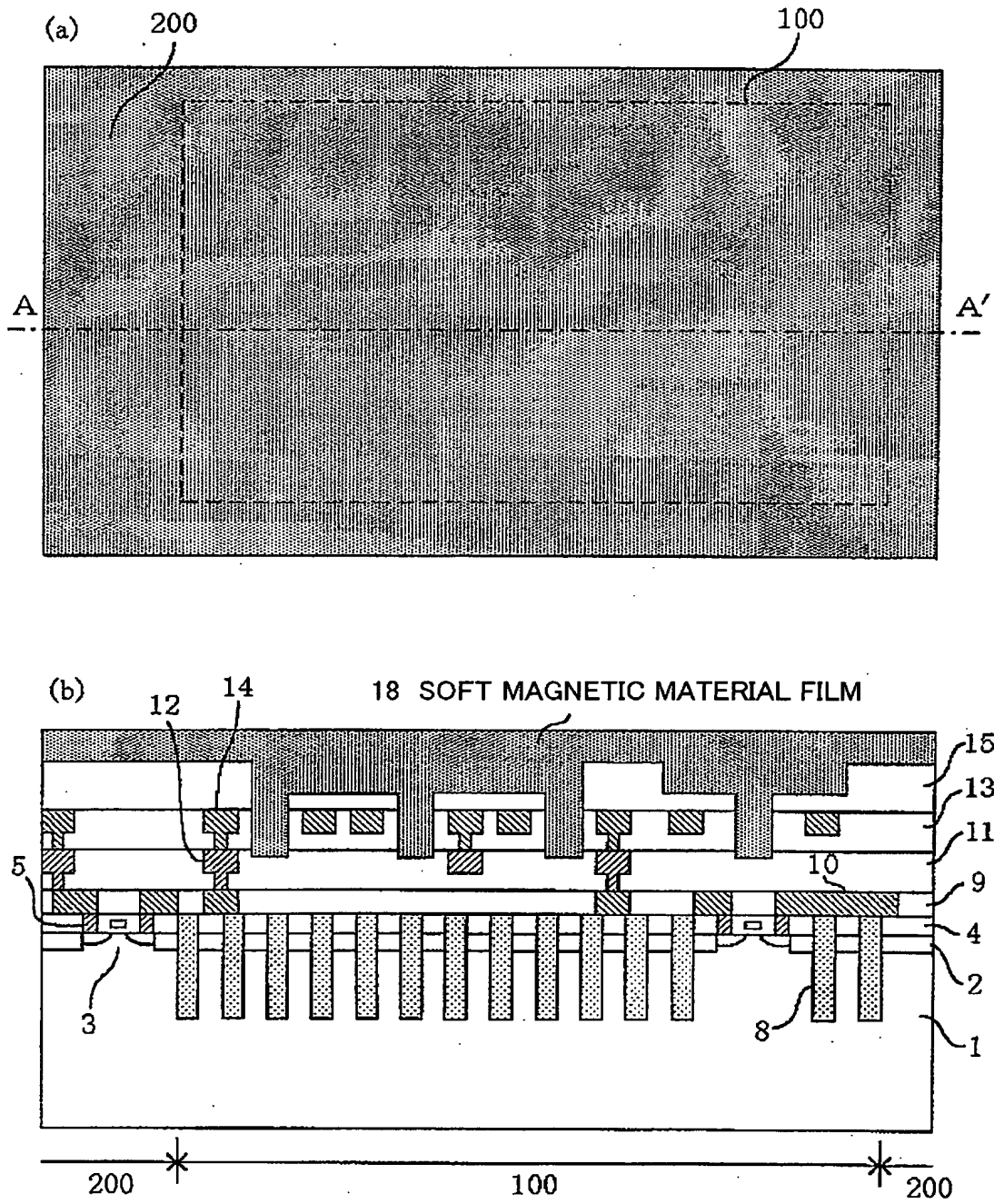


Fig. 18

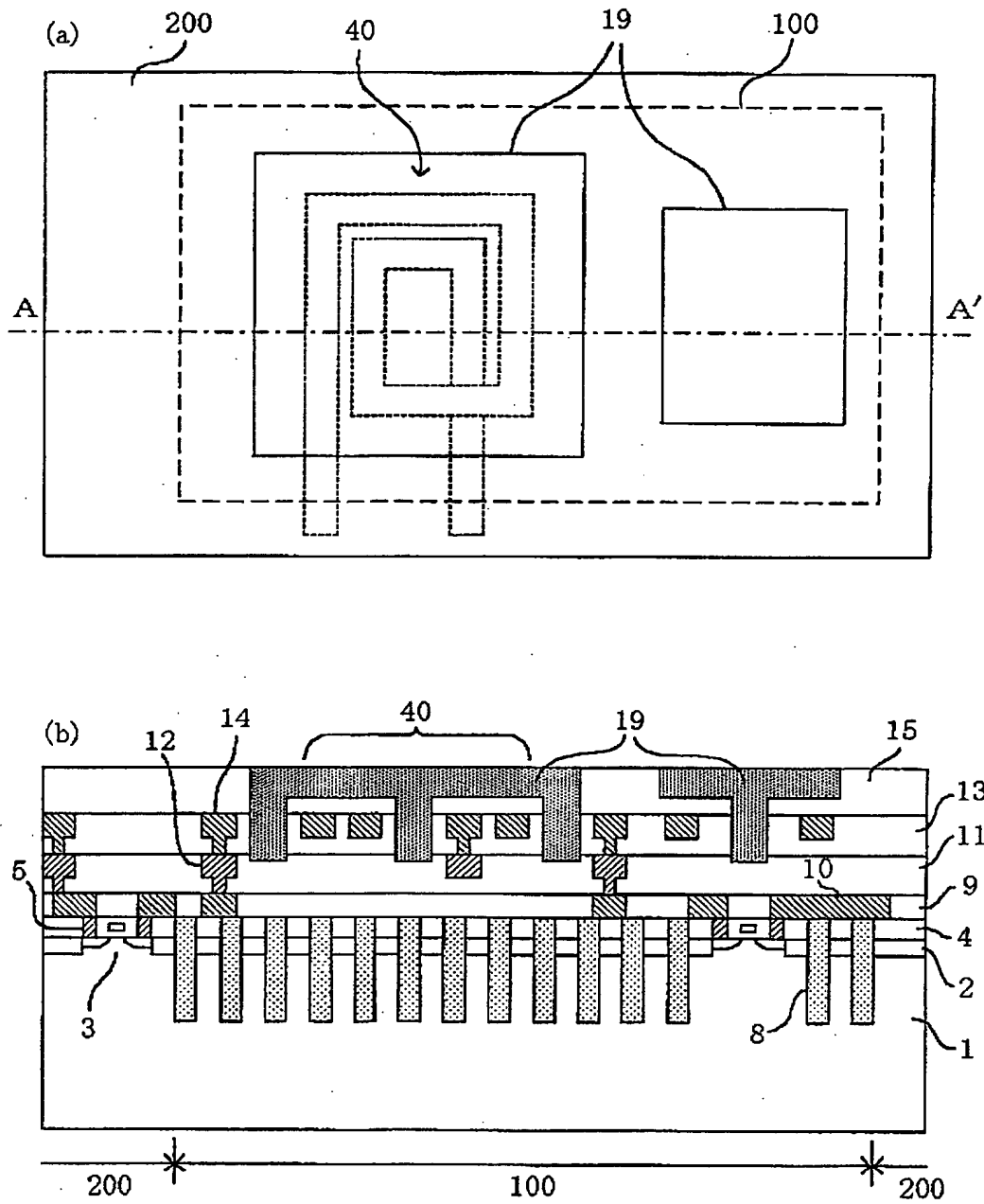


Fig. 19

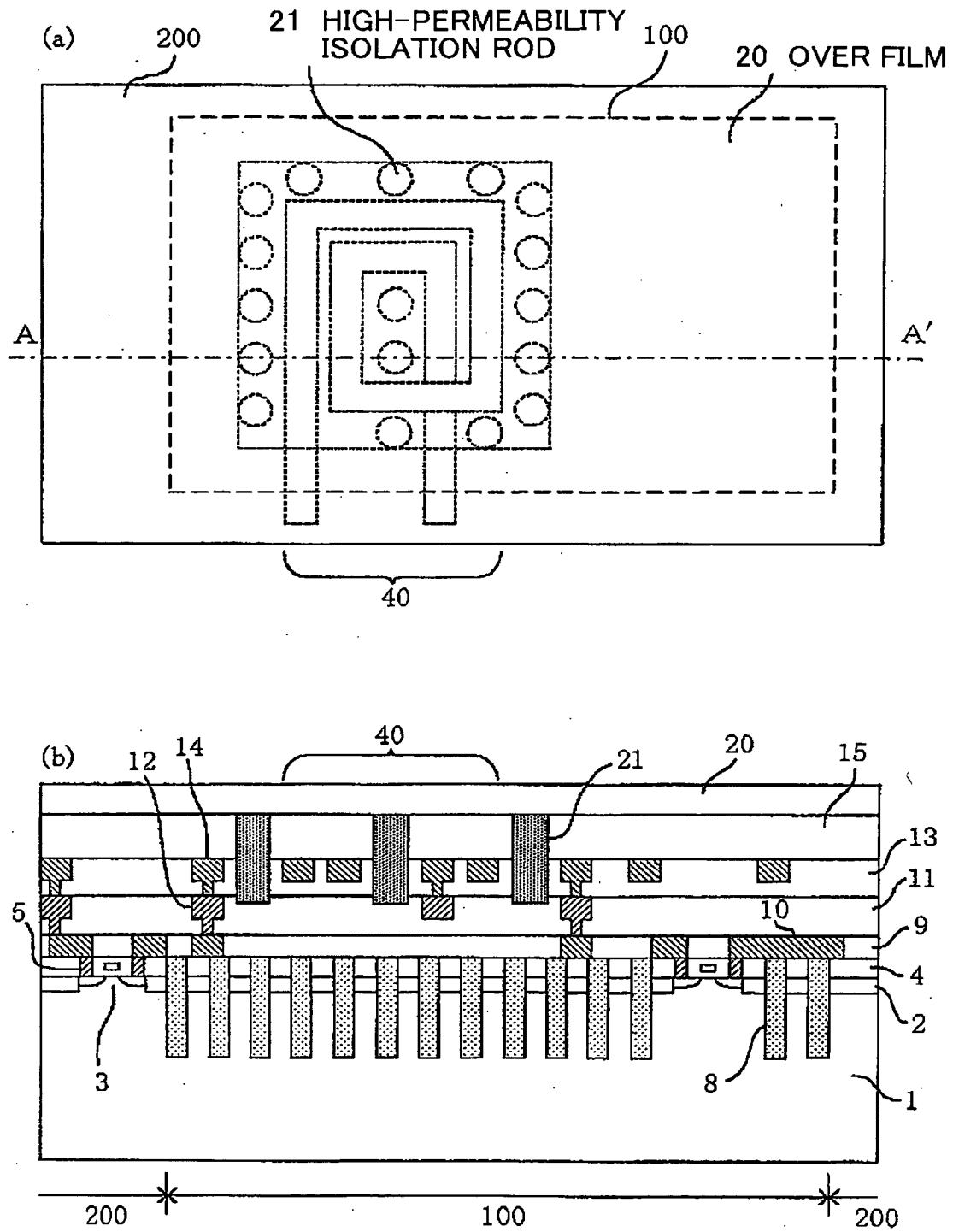
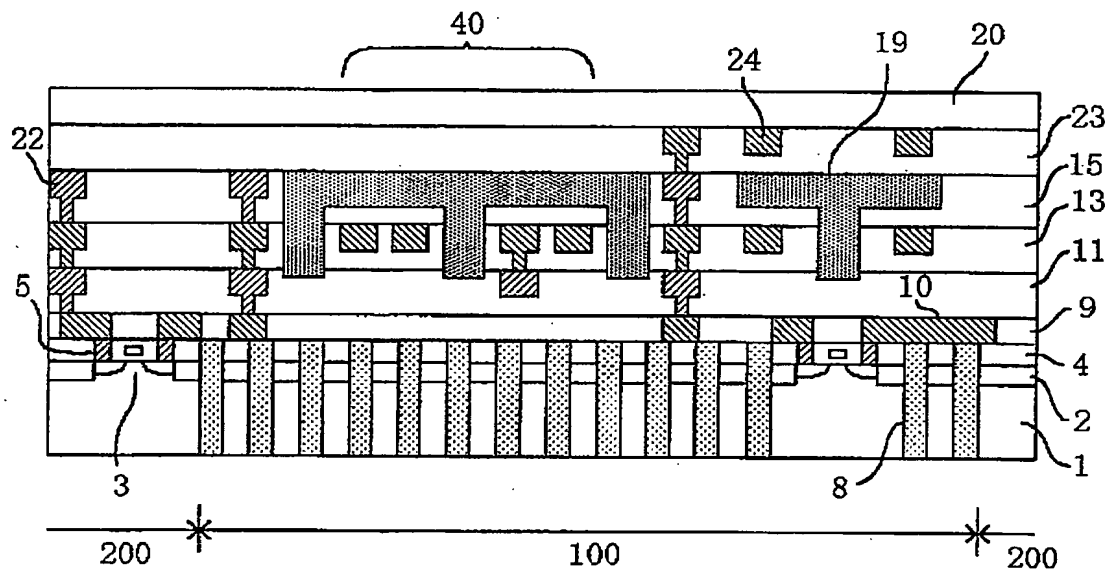


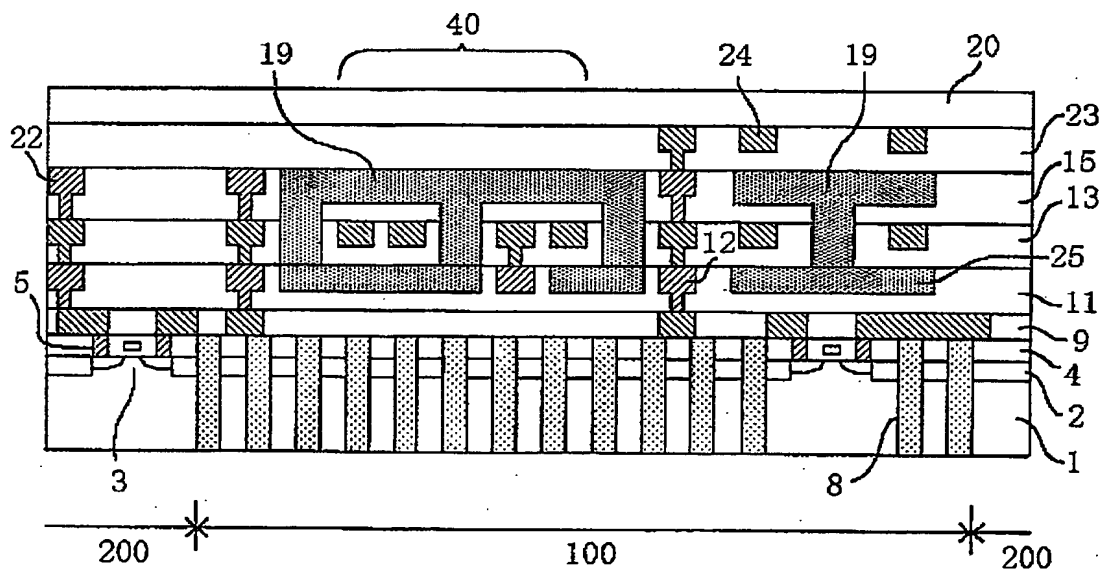


Fig. 20



22 FOURTH-LEVEL COPPER INTERCONNECT  
23 SIXTH INTERLEVEL DIELECTRIC FILM

Fig. 21



24 FIFTH-LEVEL COPPER INTERCONNECT  
25 HIGH-PERMEABILITY ISOLATION PLANE

Fig. 22

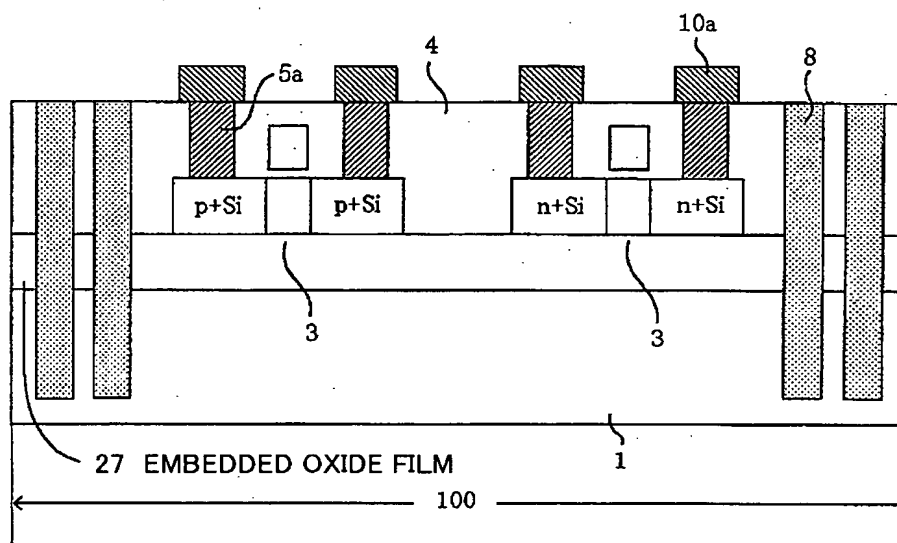
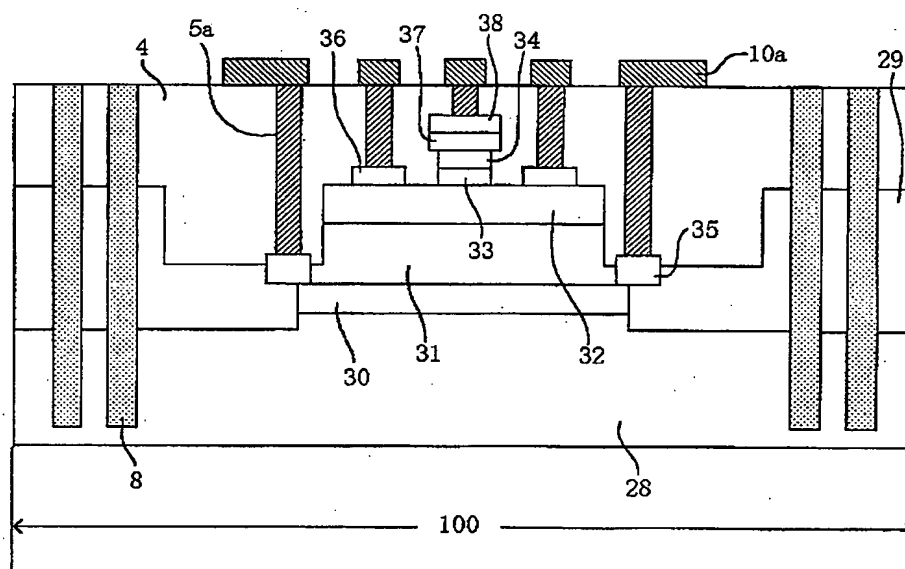


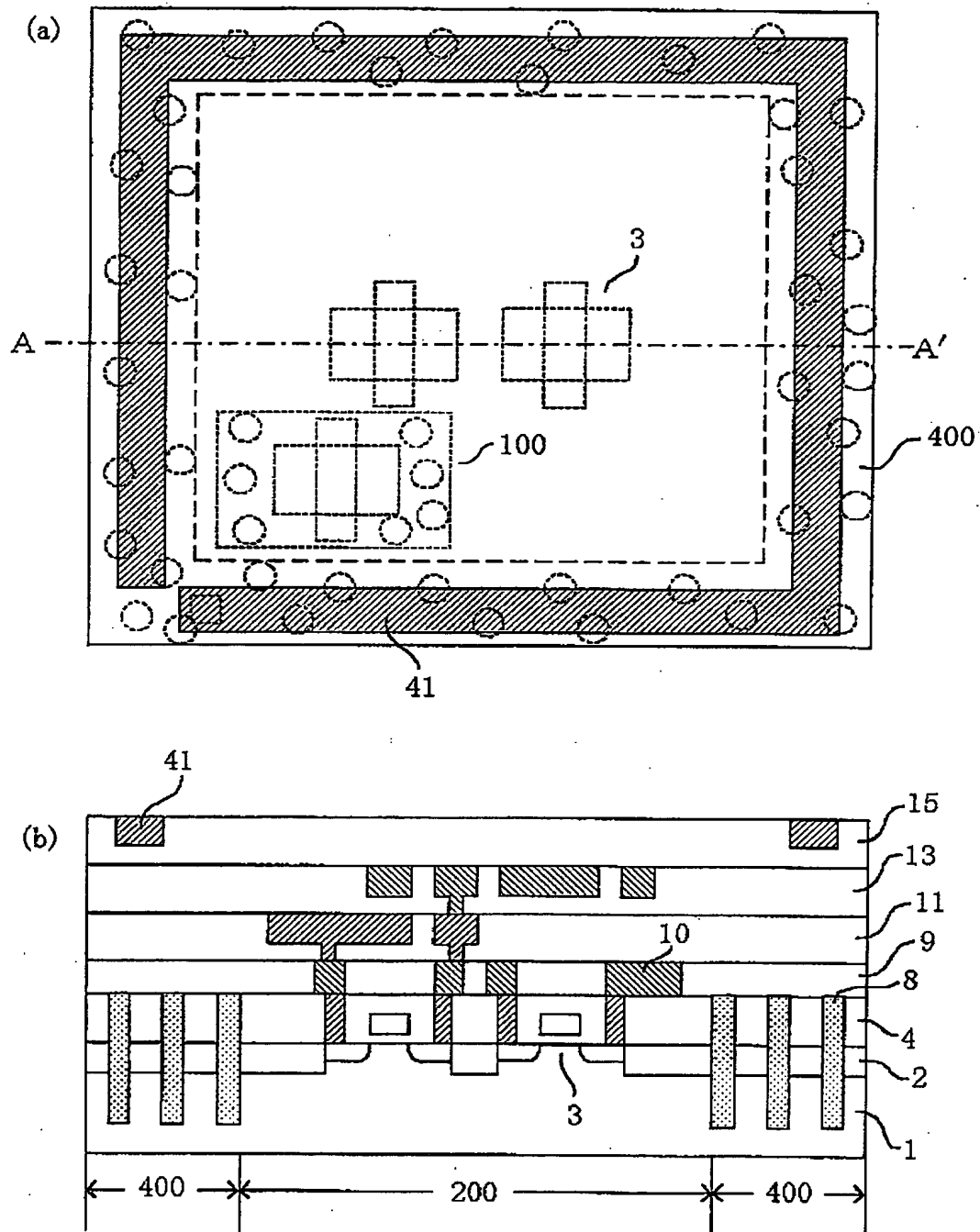
Fig. 23



28 SEMI-INSULATING GAAS SUBSTRATE  
 29 H<sup>+</sup>-DOPED HIGH RESISTANCE AREA  
 30 N<sup>+</sup>-GAAS LAYER  
 31 N<sup>-</sup>-GAAS LAYER  
 32 P<sup>+</sup>-GAAS LAYER

33 N<sup>-</sup>-ALGAAS LAYER  
 34 N-INGAAS LAYER  
 35 AU/NI/AUGE LAYER  
 36, 38 AU/PT LAYER  
 37 WSI LAYER

Fig. 24



41 ON-CHIP ANTENNA INTERCONNECT  
400 PERIPHERAL HIGH-RESISTANCE AREA

Fig. 25

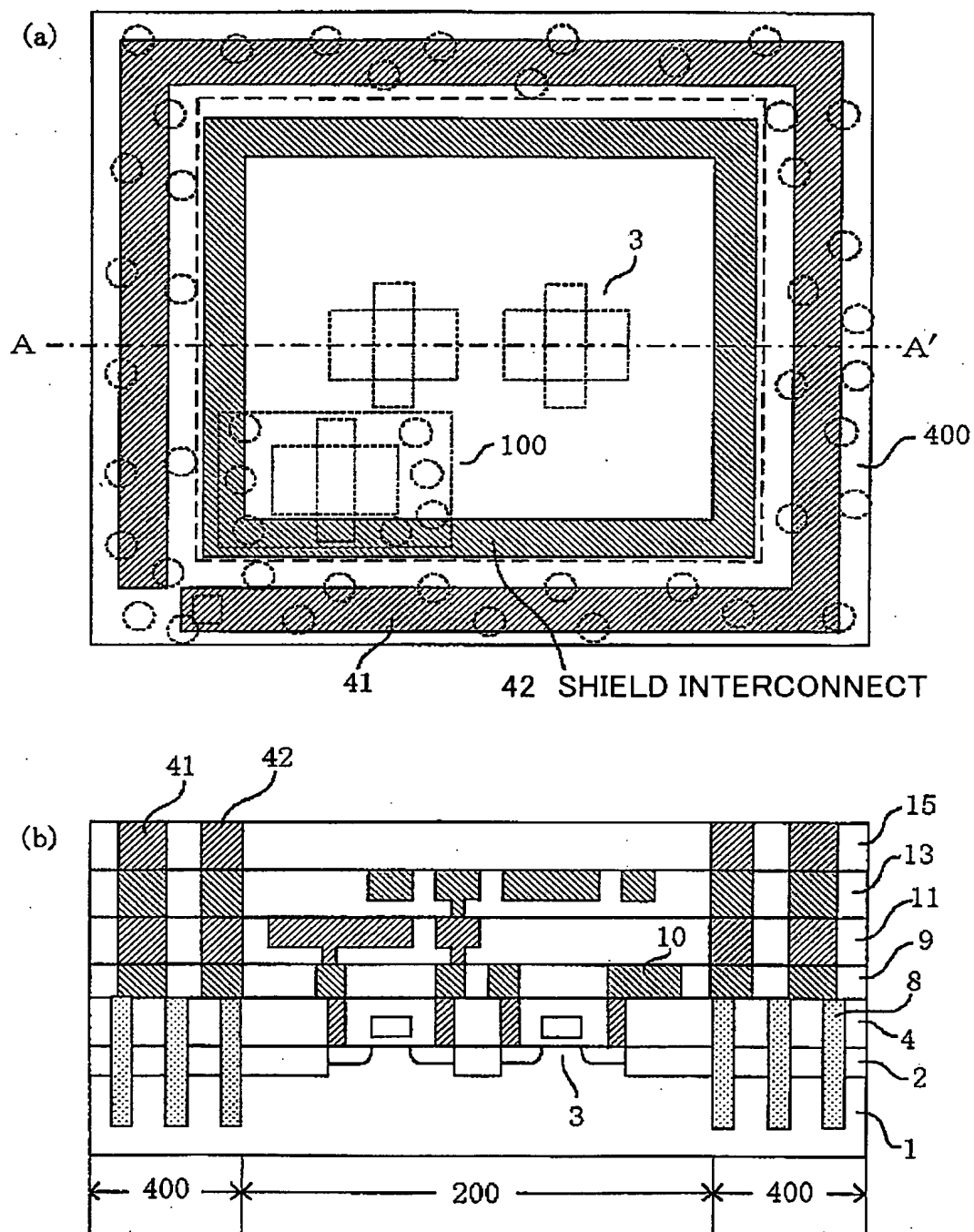
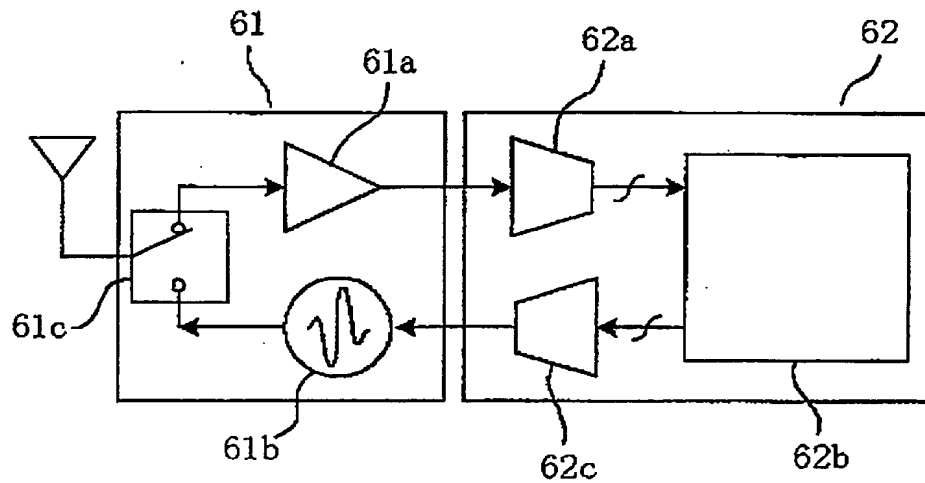


Fig. 26



- 61 RF COMMUNICATION CIRCUIT AREA
- 61A LNA
- 61B TRANSMISSION SIGNAL GENERATING CIRCUIT
- 61C SWITCH CIRCUIT
- 62 DIGITAL BASEBAND
- 62A A/D CIRCUIT
- 62B DIGITAL SIGNAL PROCESSING CIRCUIT
- 62C D/A CIRCUIT

Fig. 27

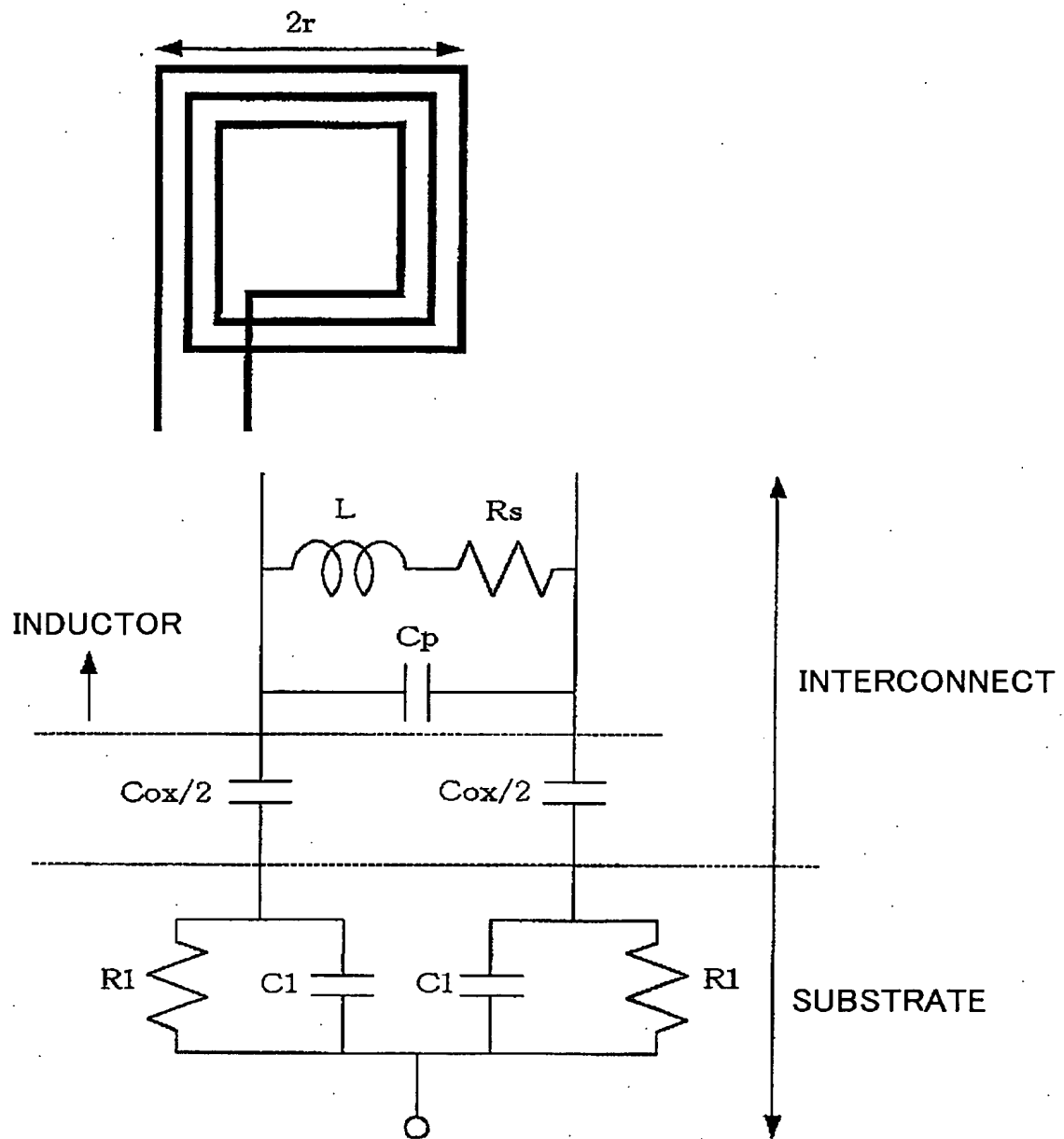


Fig. 28

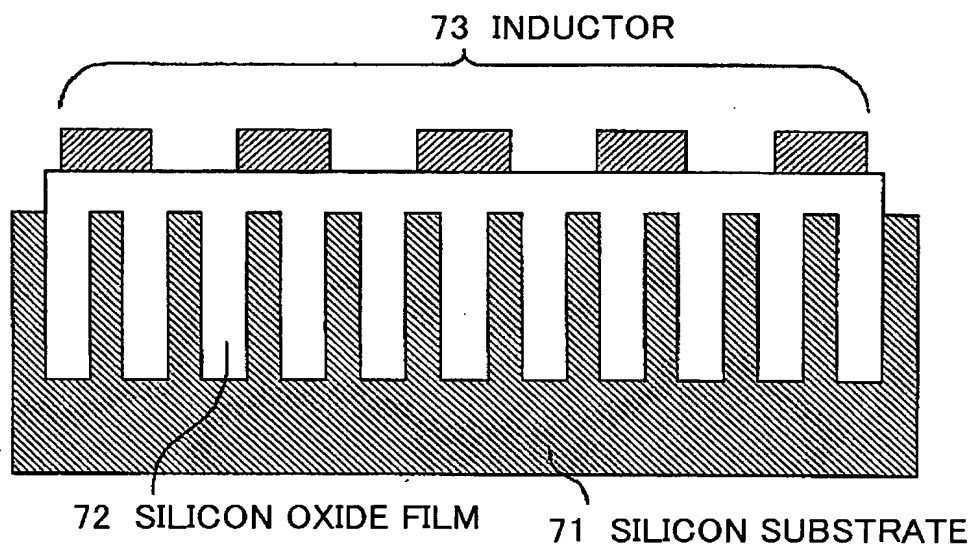


Fig. 29

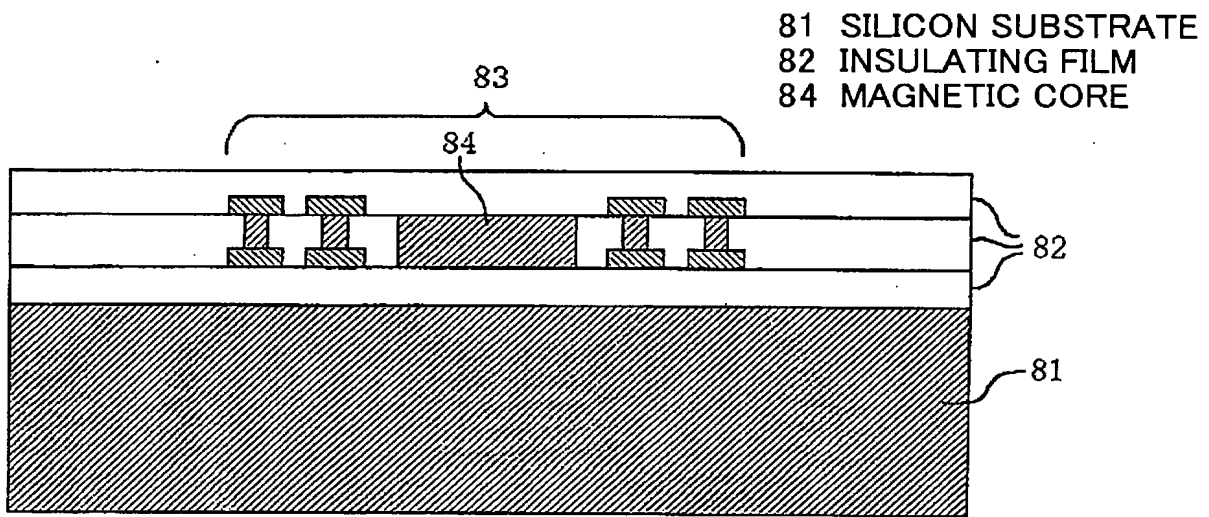




Fig. 30

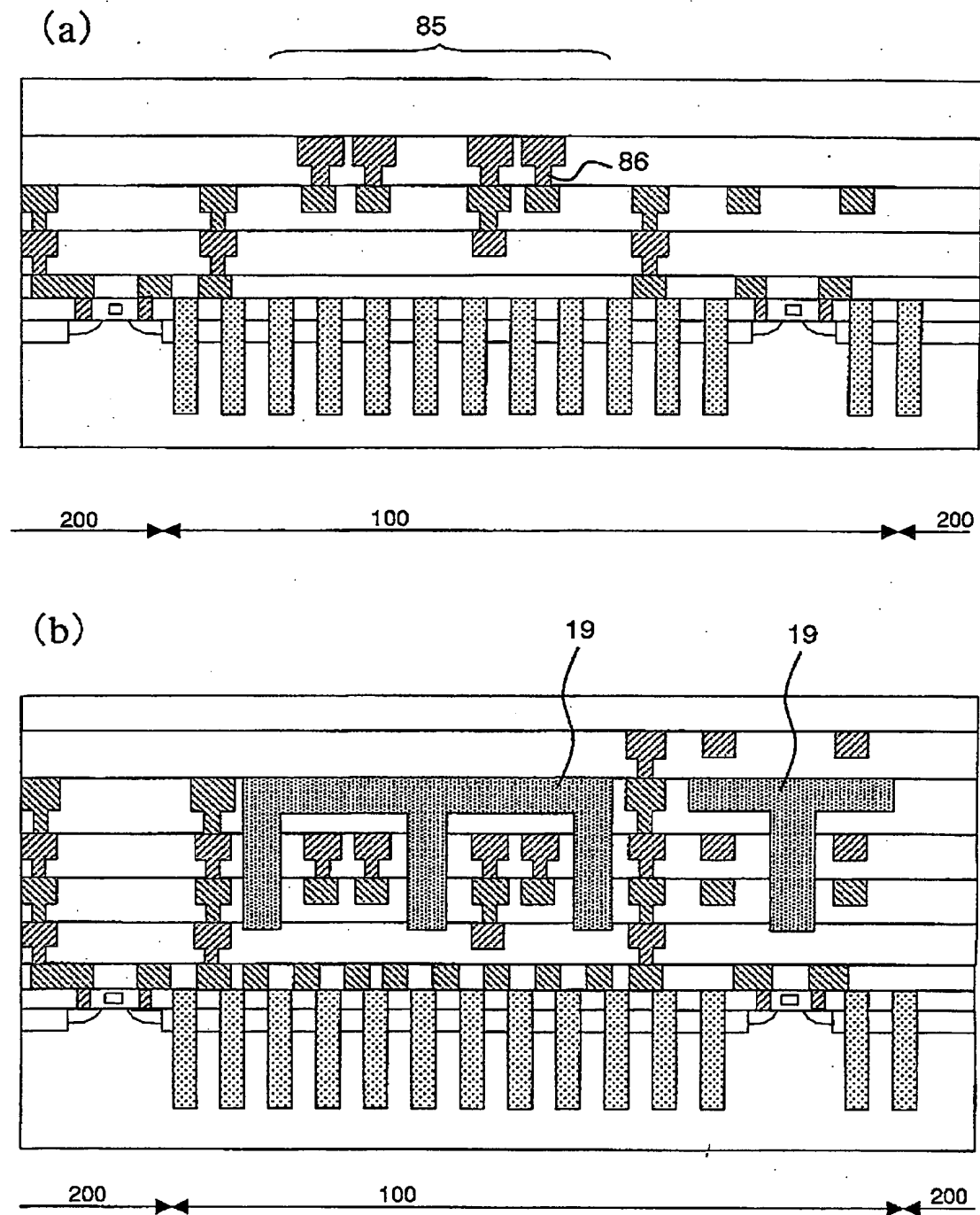


Fig. 31

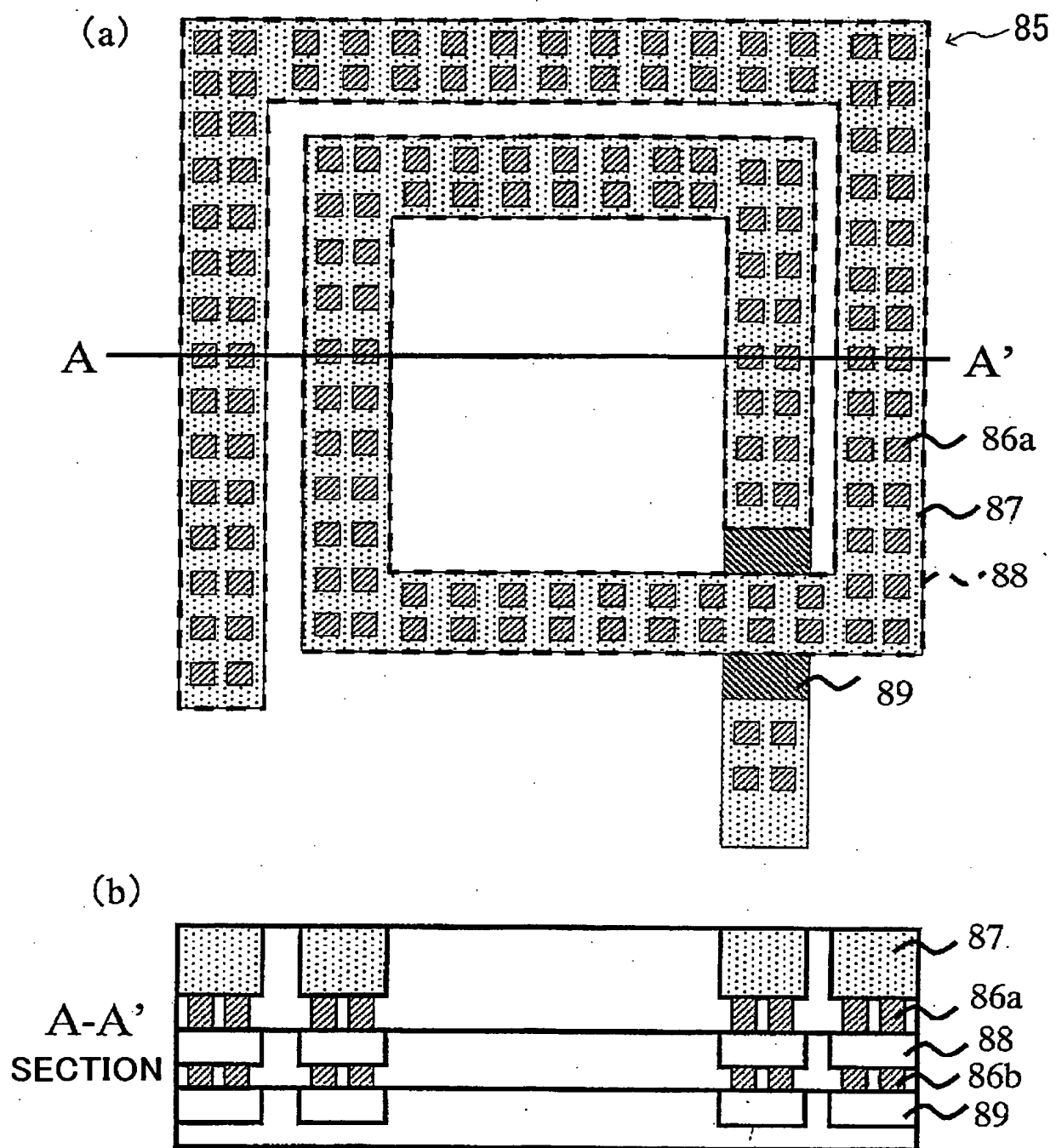


Fig. 32

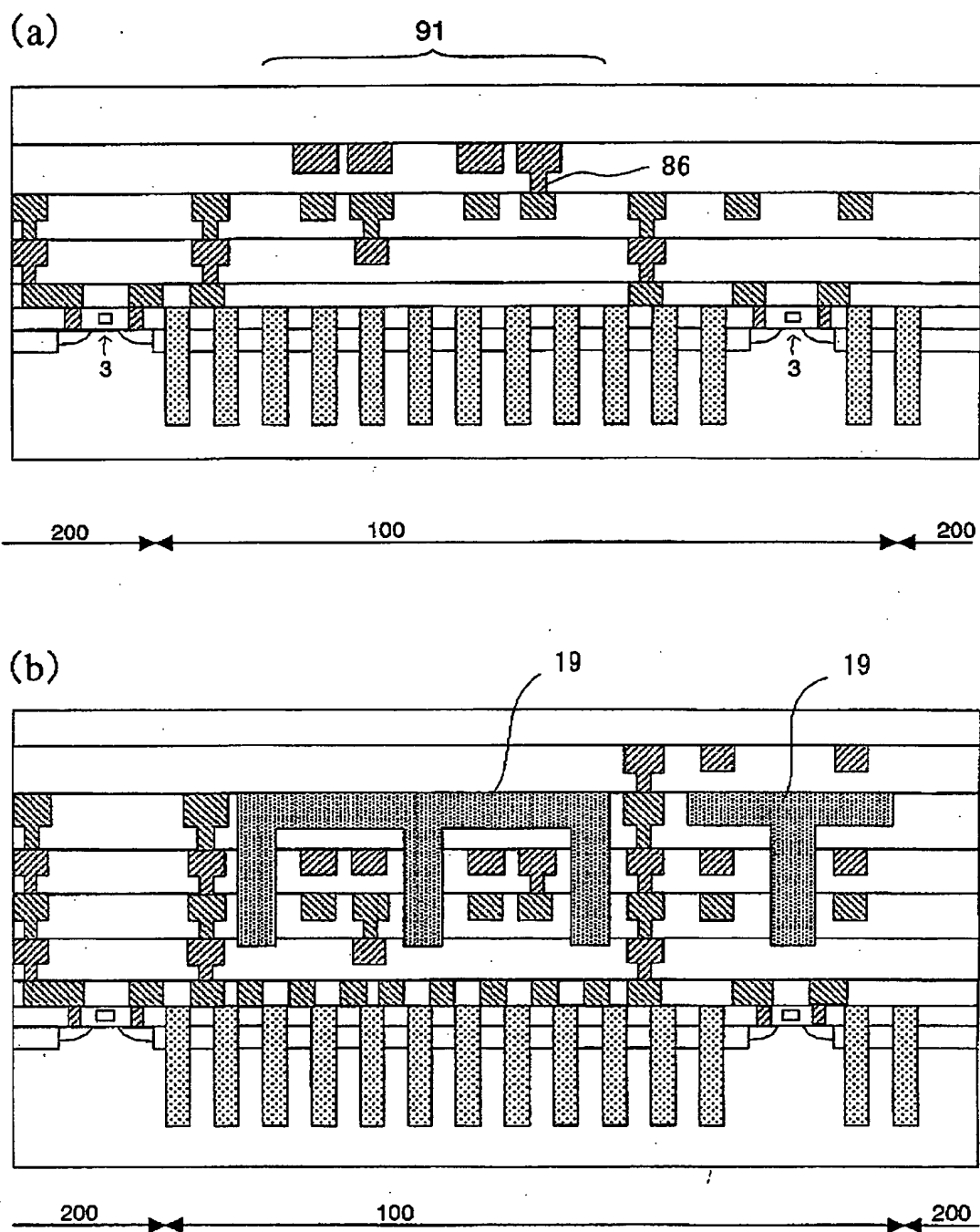


Fig. 33

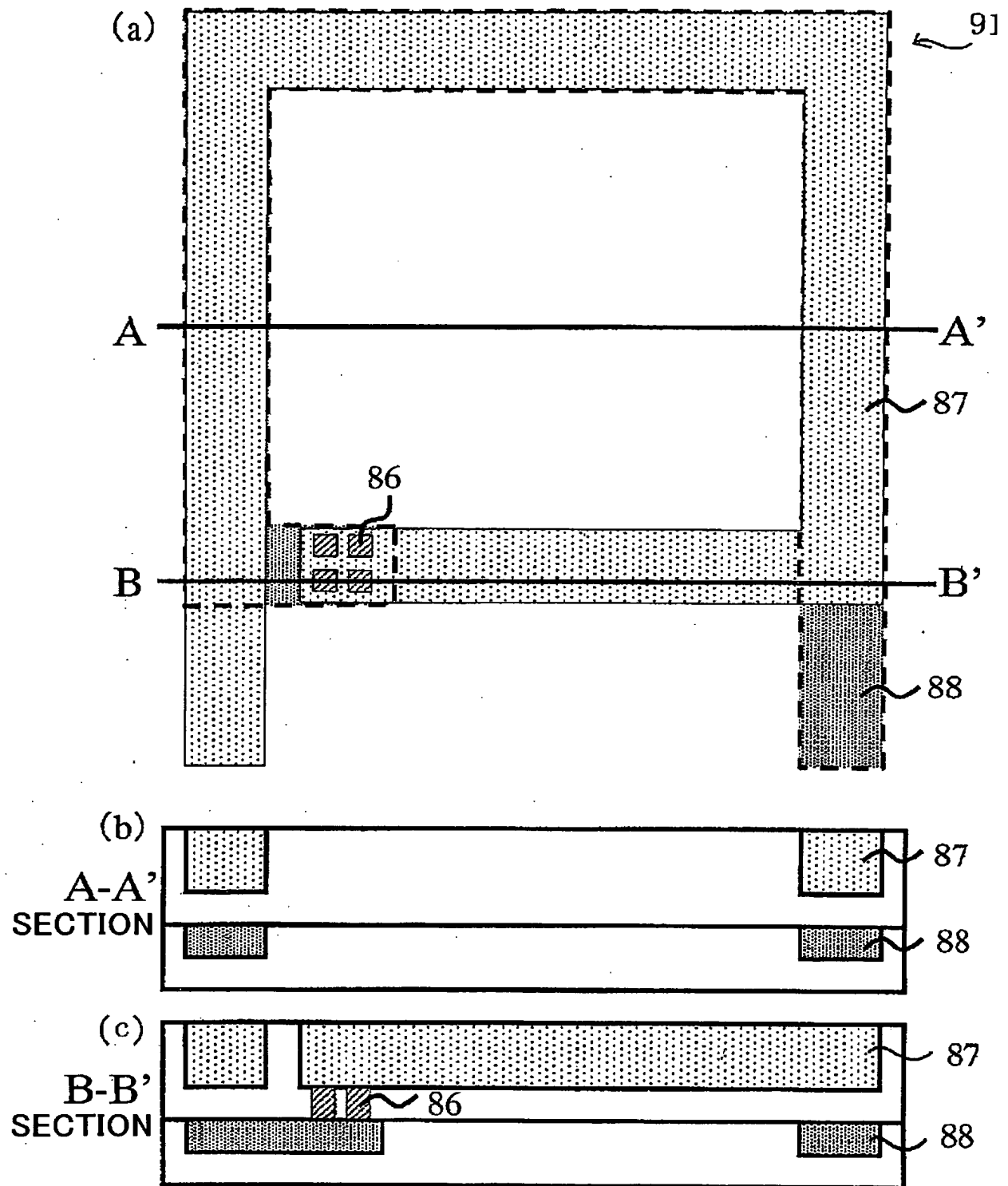


Fig. 34

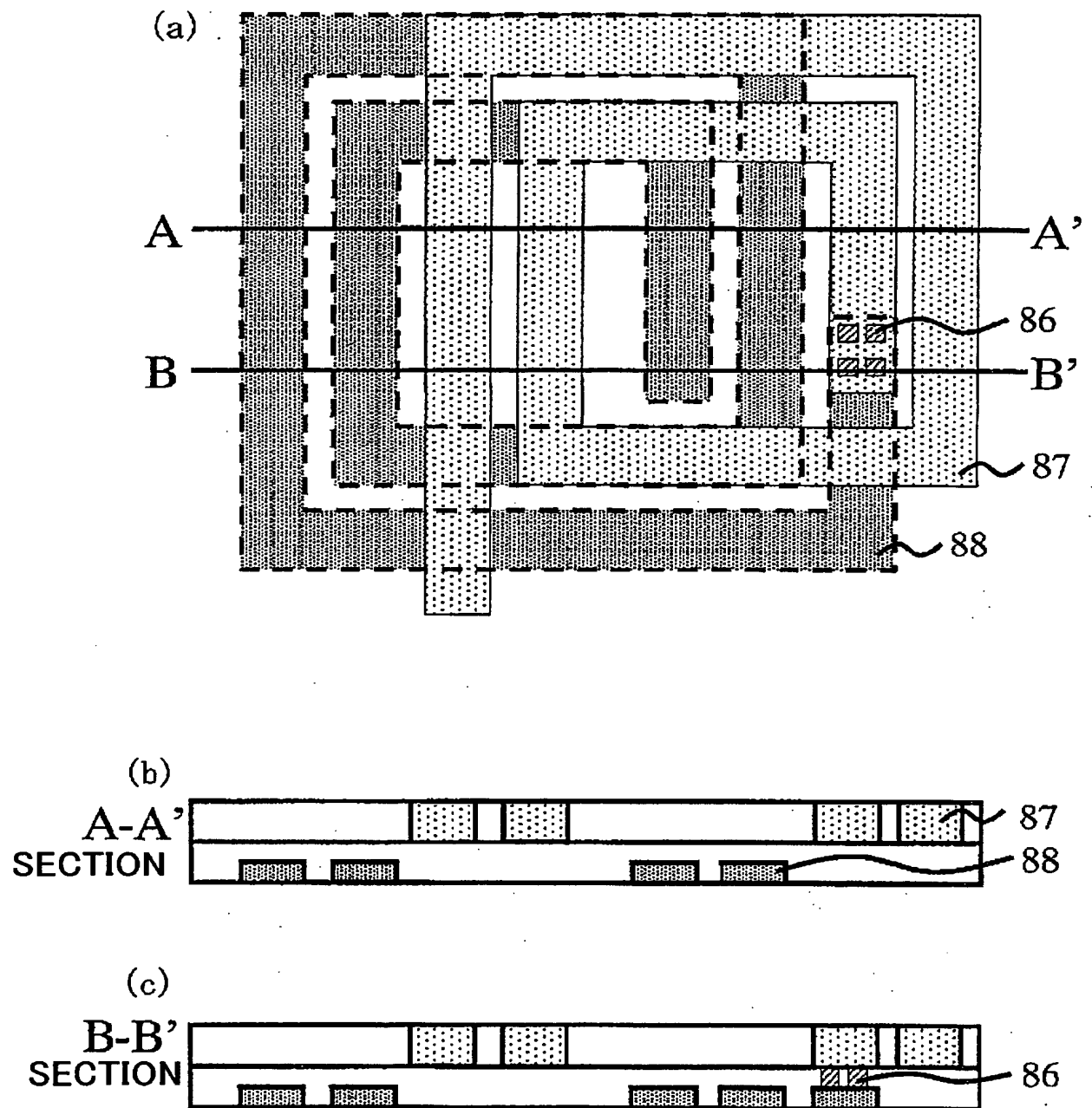


Fig. 35

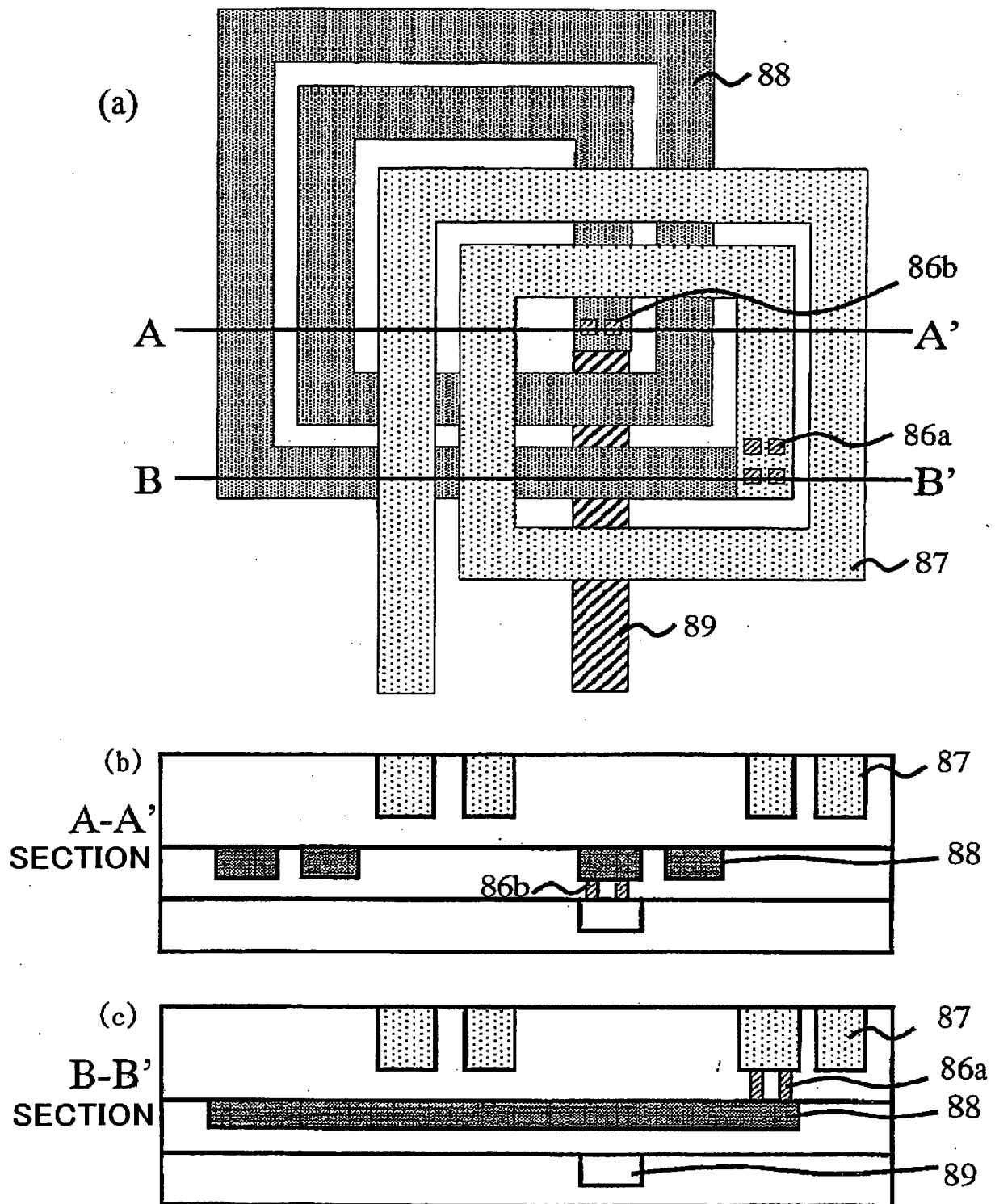


Fig. 36

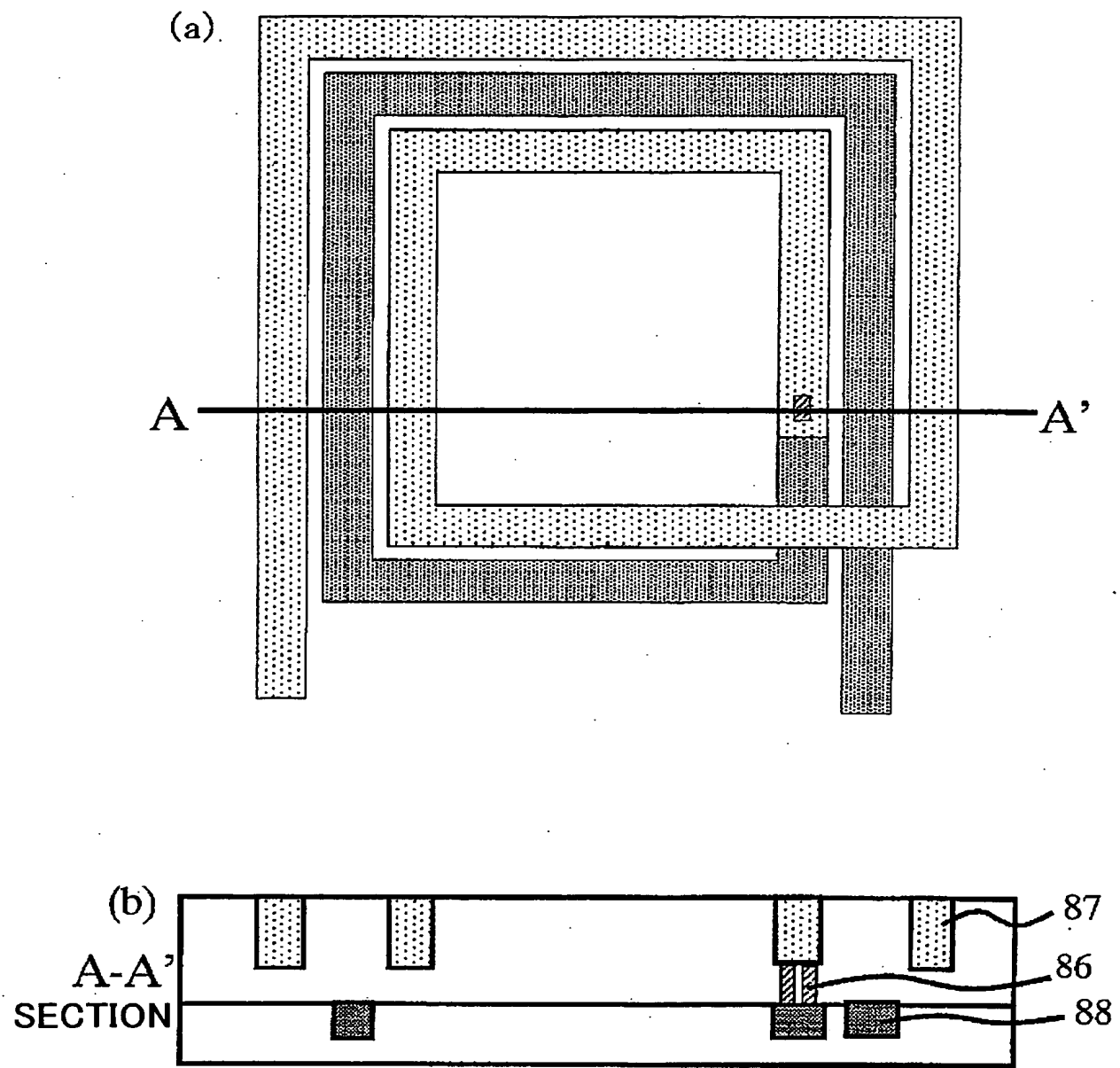


Fig. 37

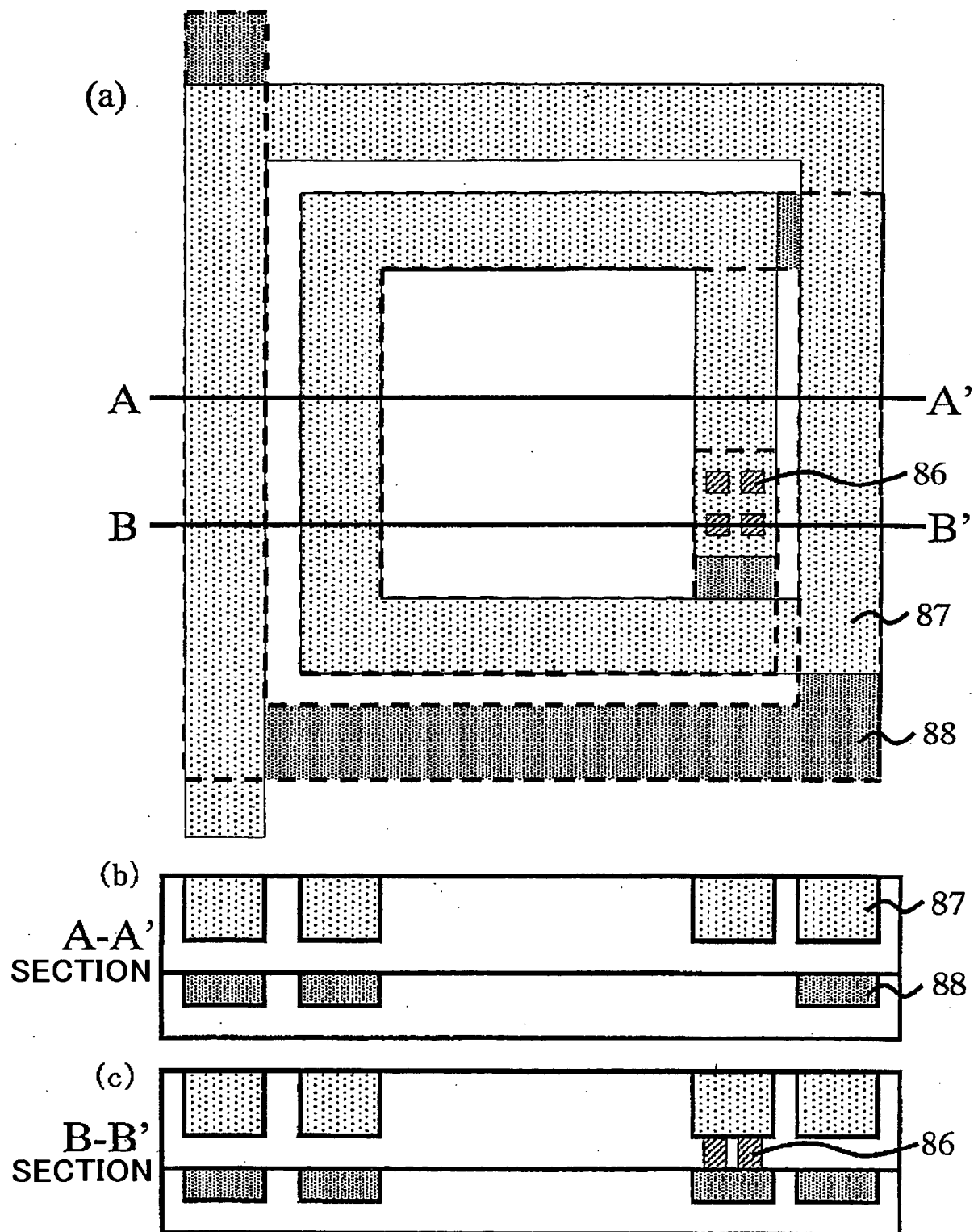




Fig. 38

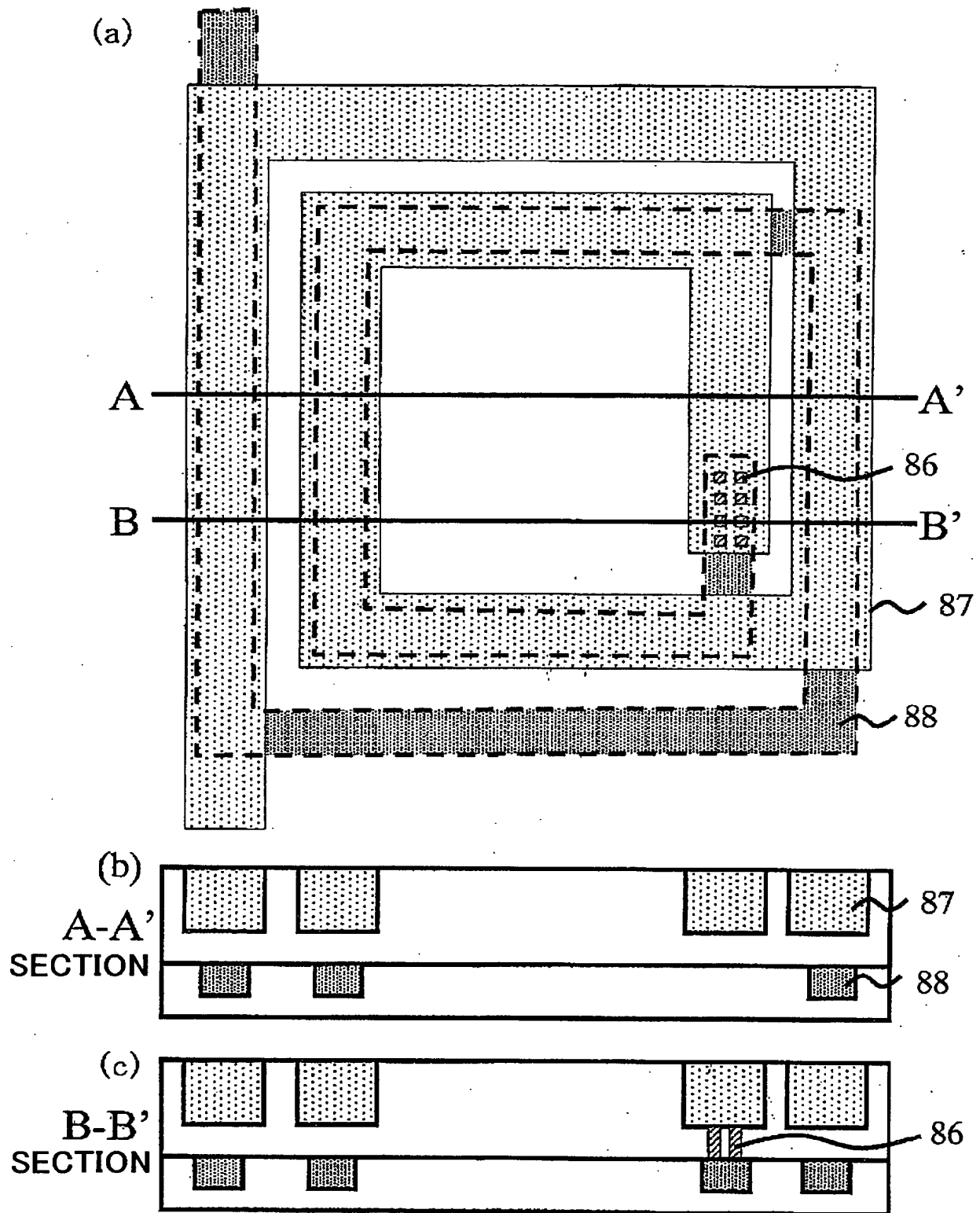


Fig. 39

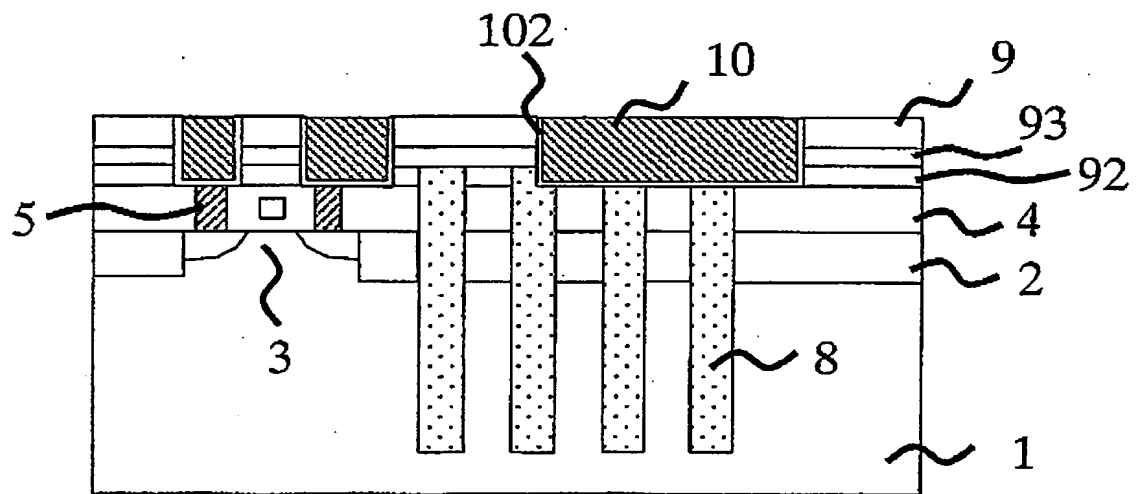


Fig. 40

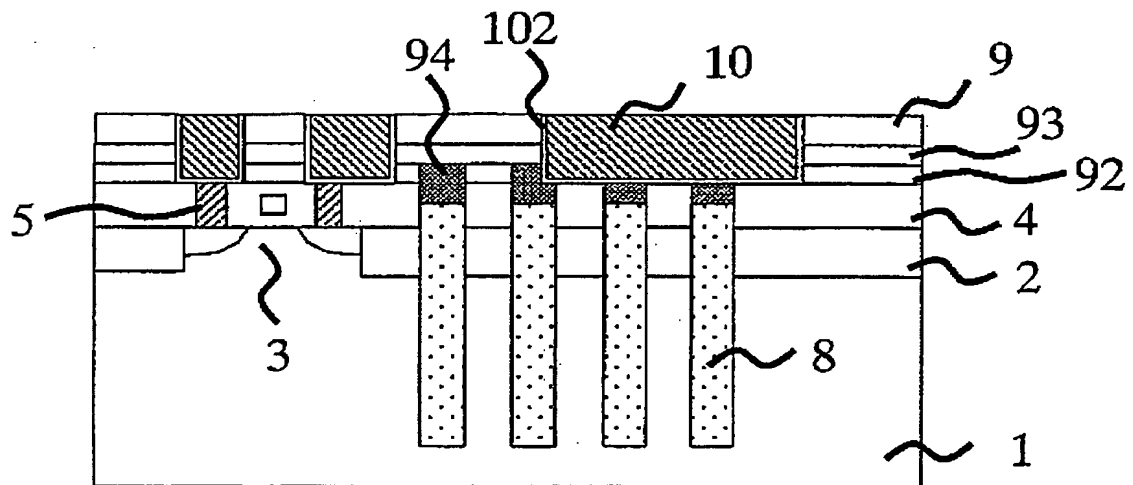


Fig. 41

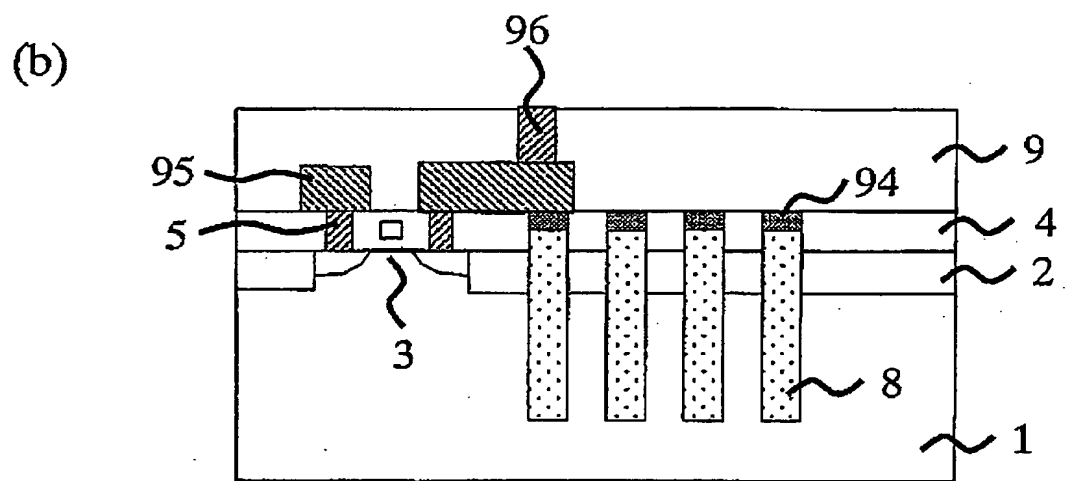
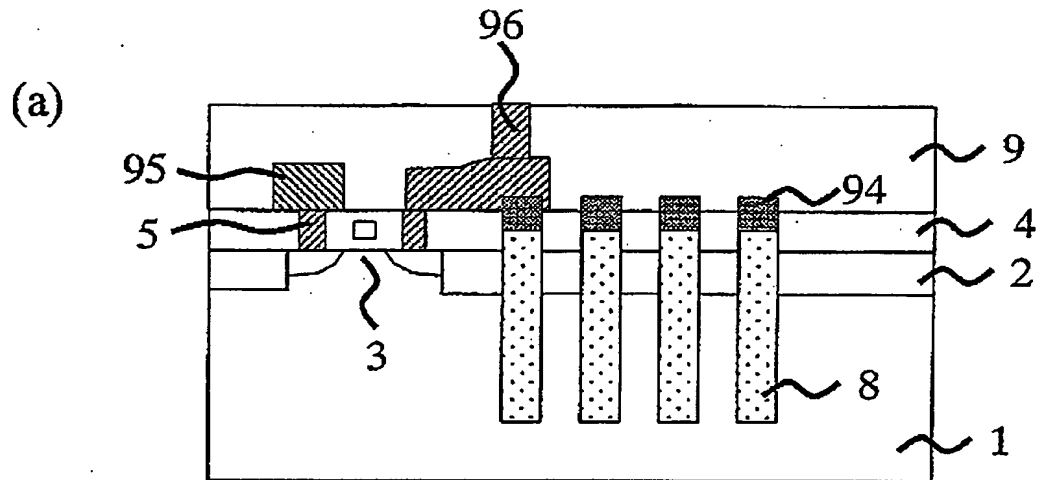


Fig. 42

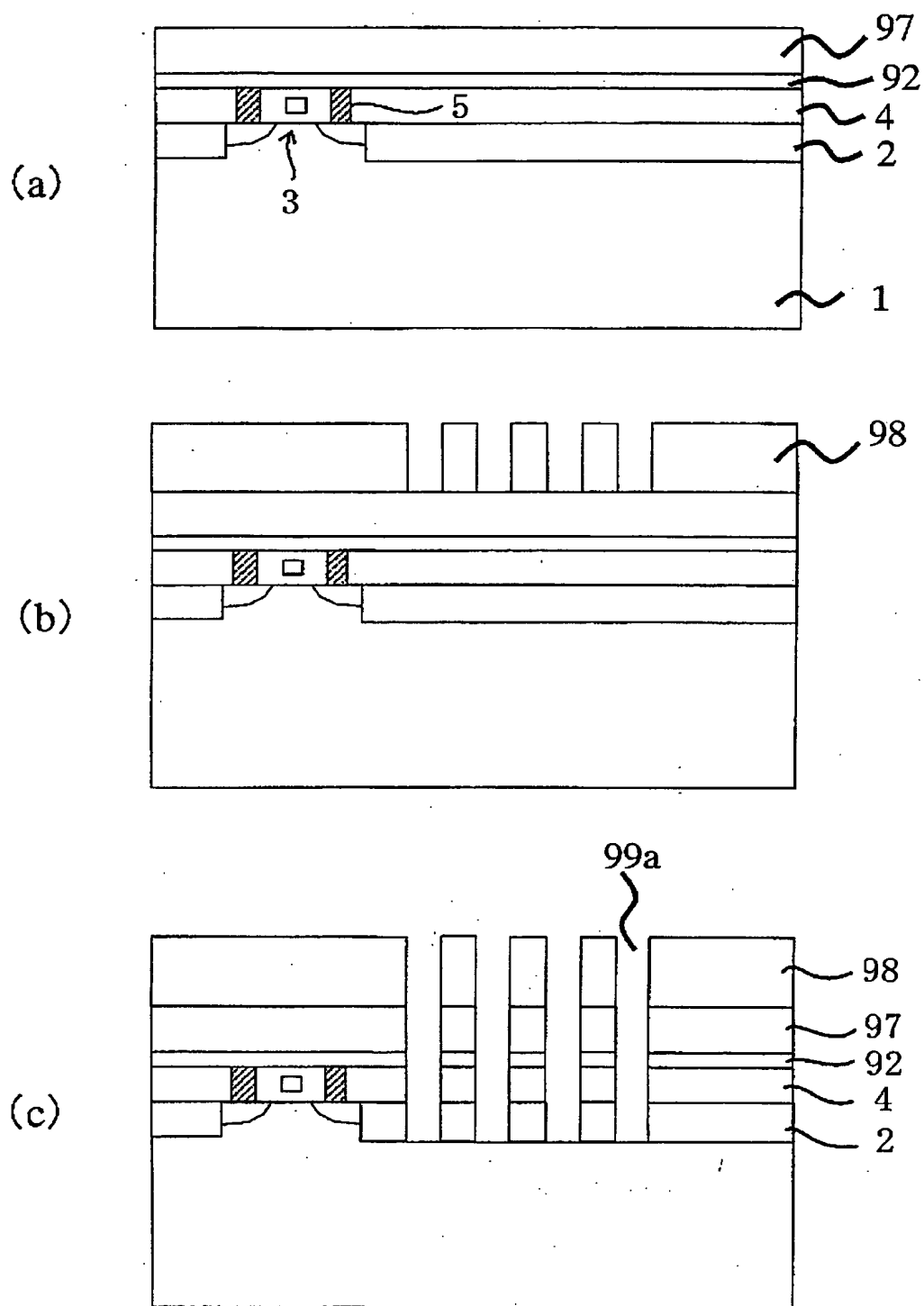


Fig. 43

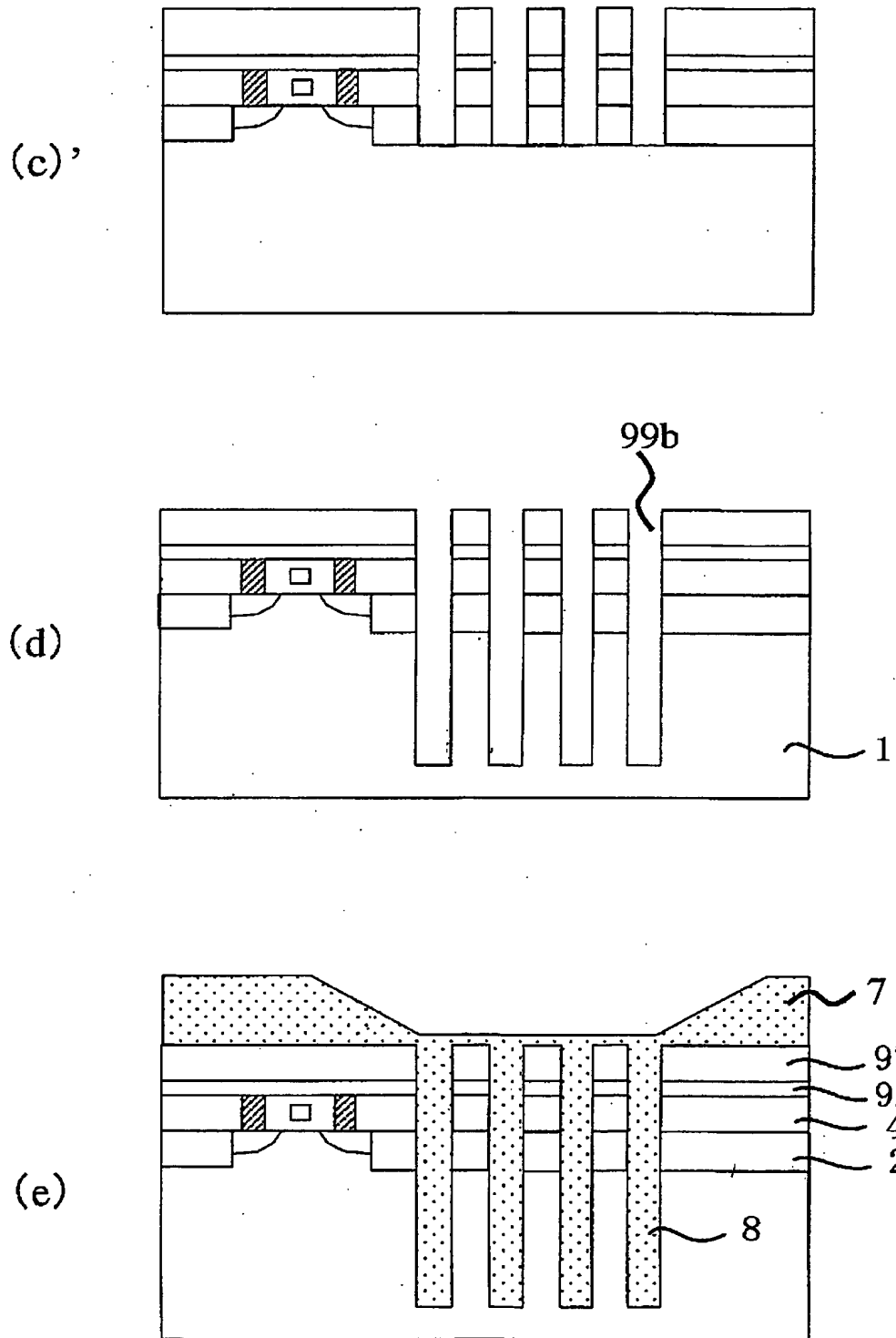


Fig. 44

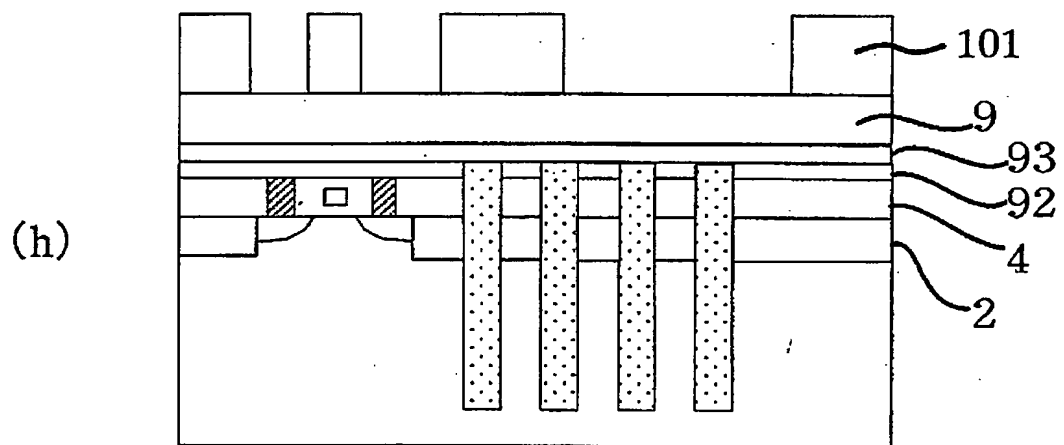
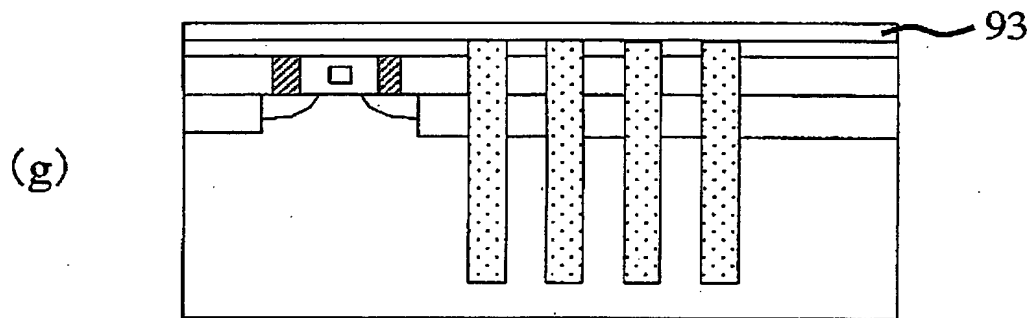
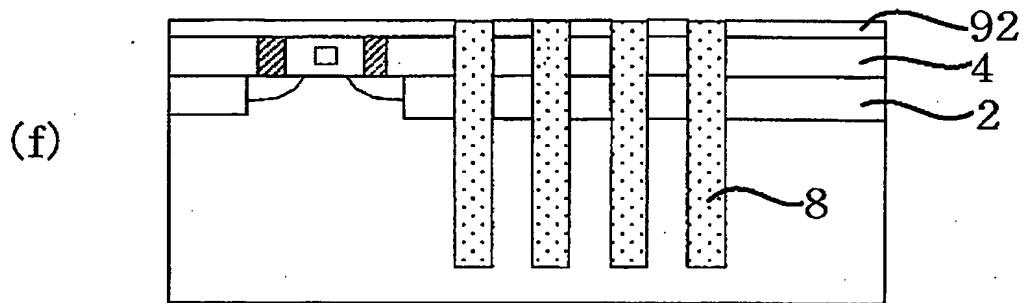


Fig. 45

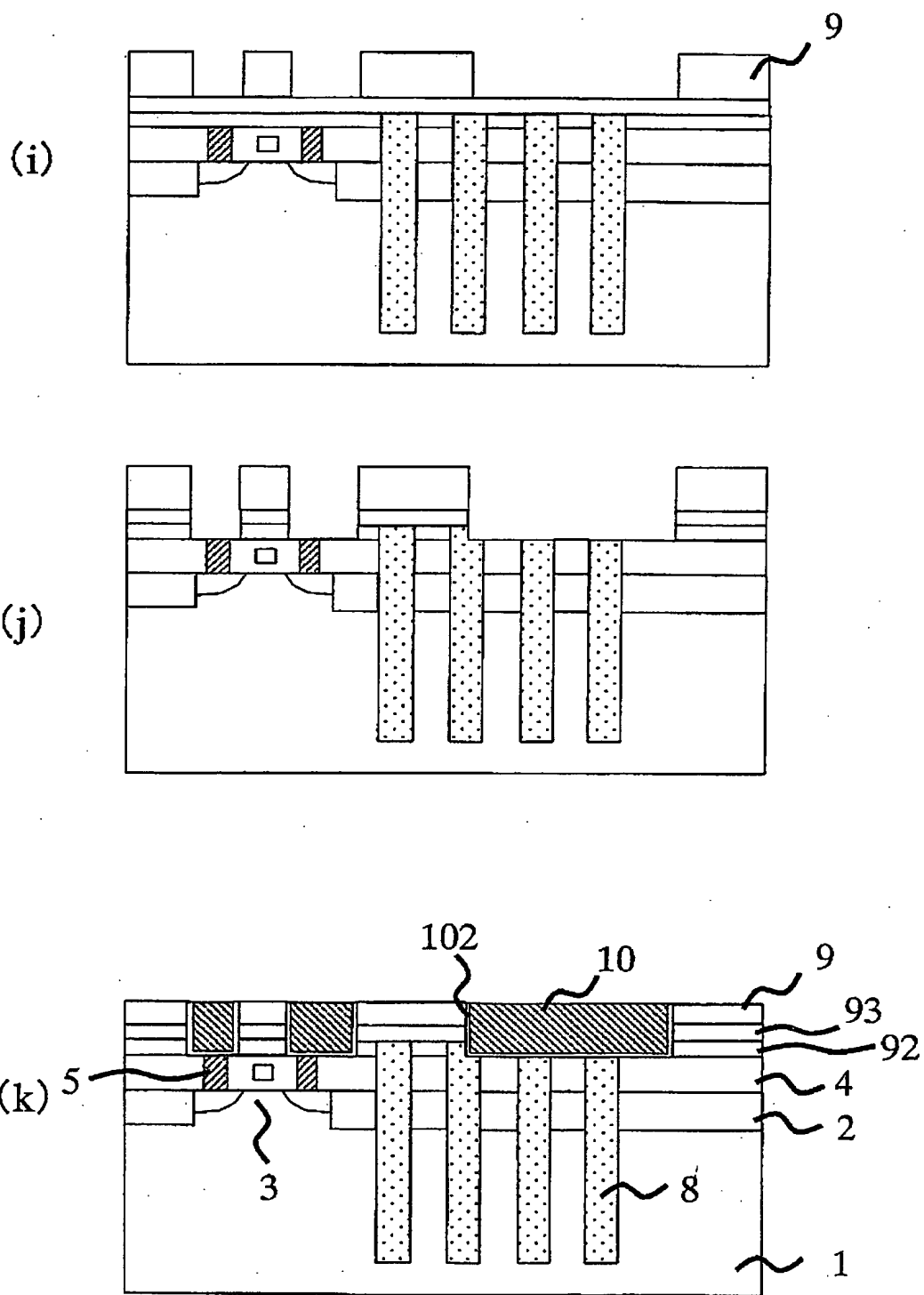


Fig. 46

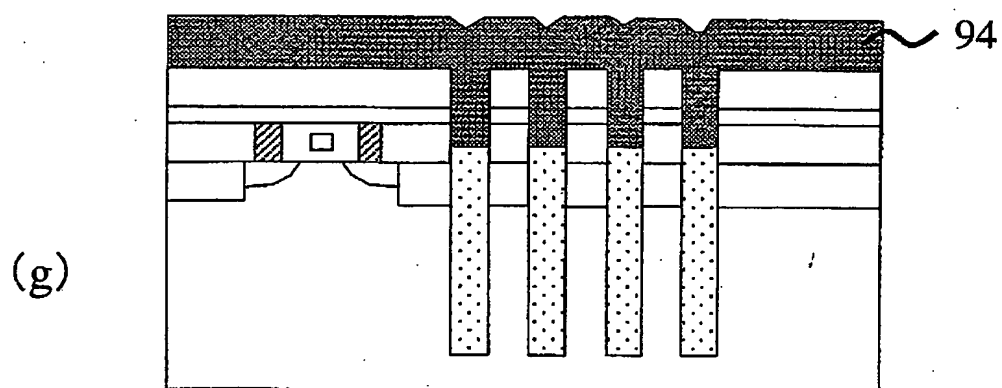
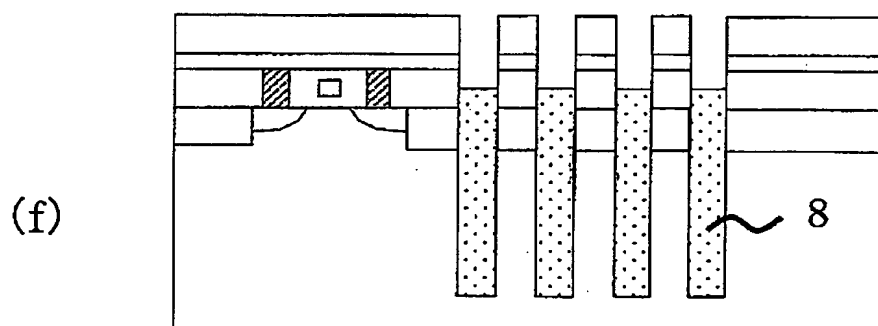
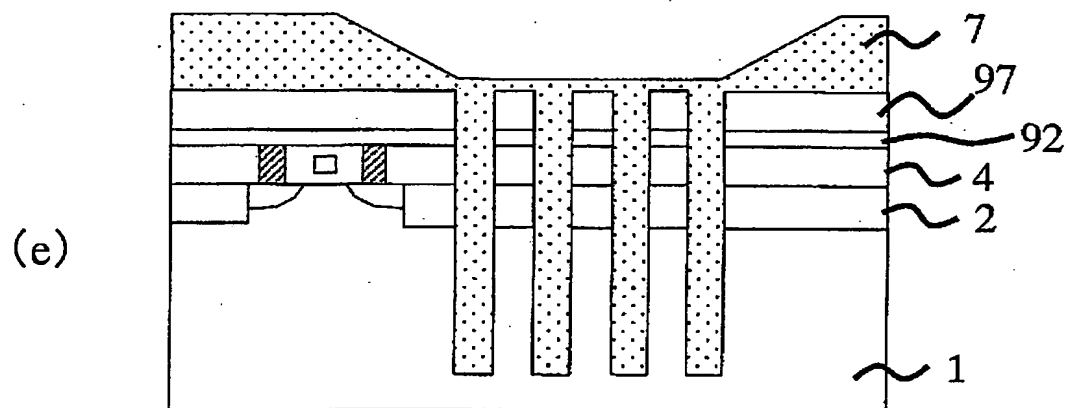




Fig. 47

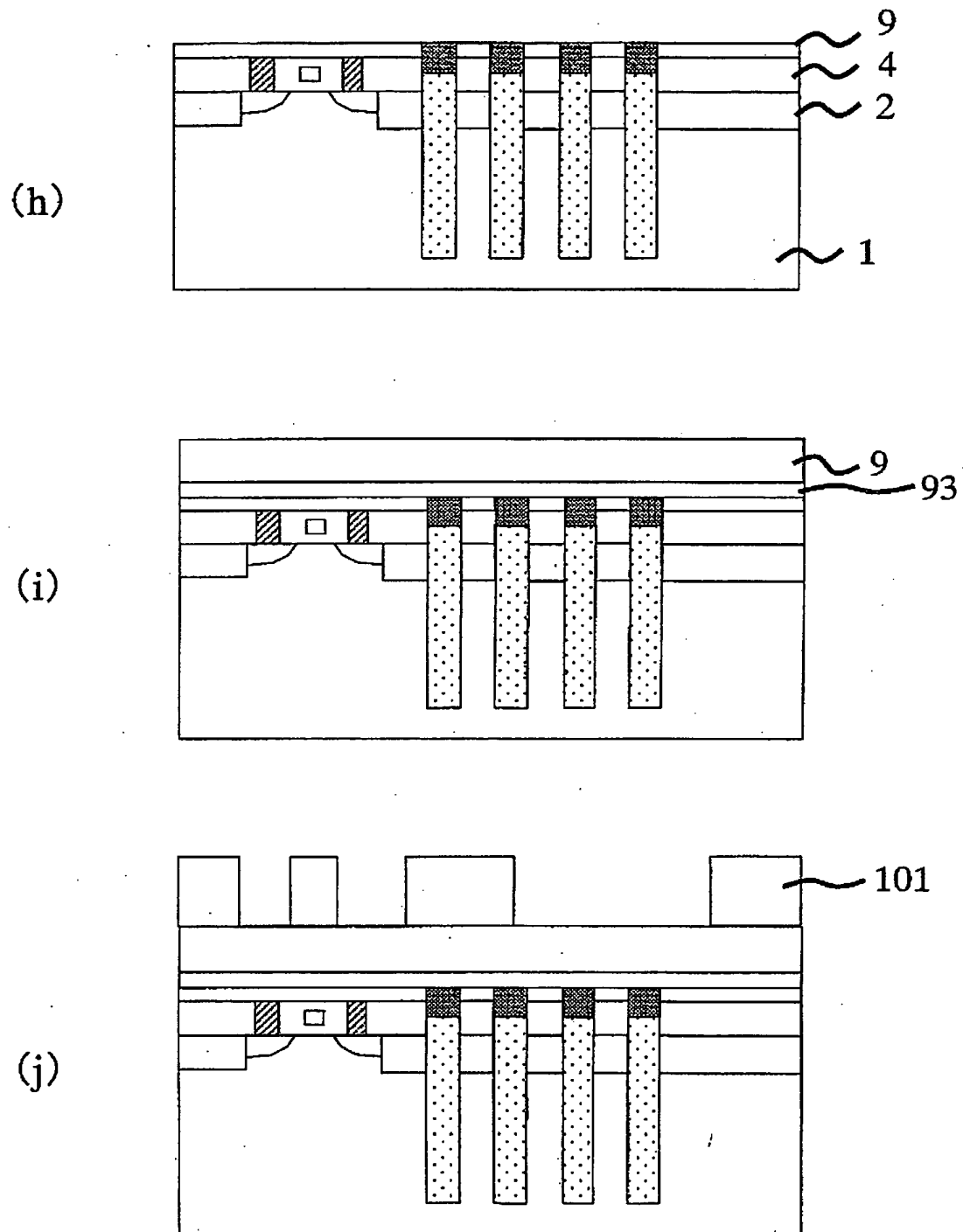


Fig. 48

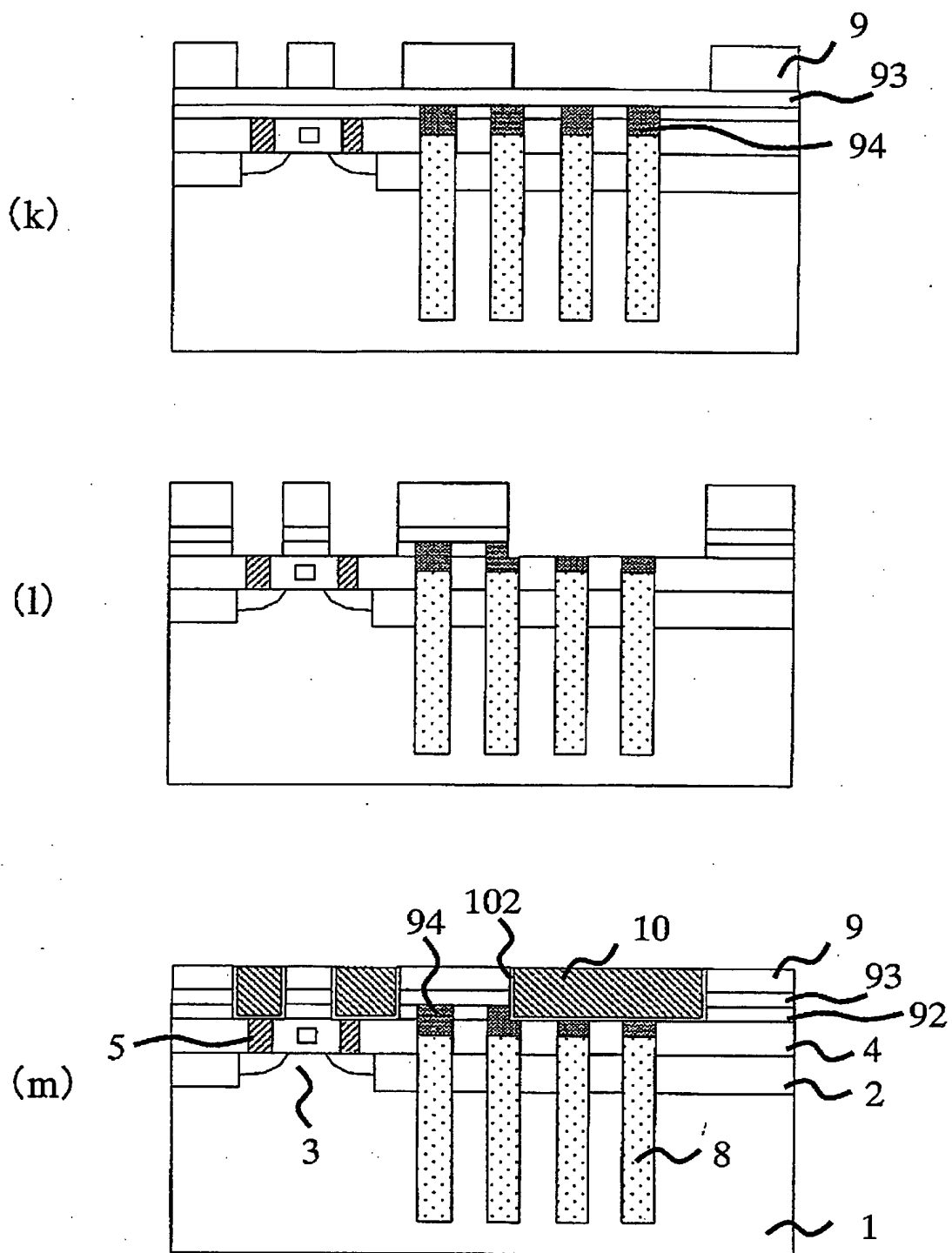


Fig. 49

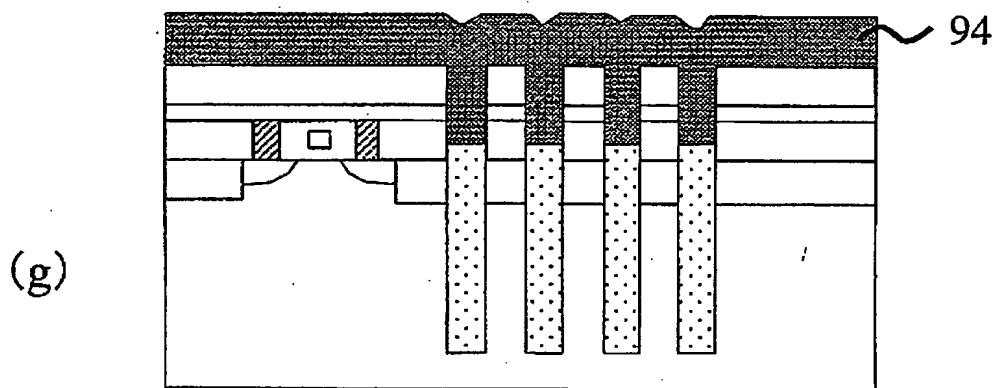
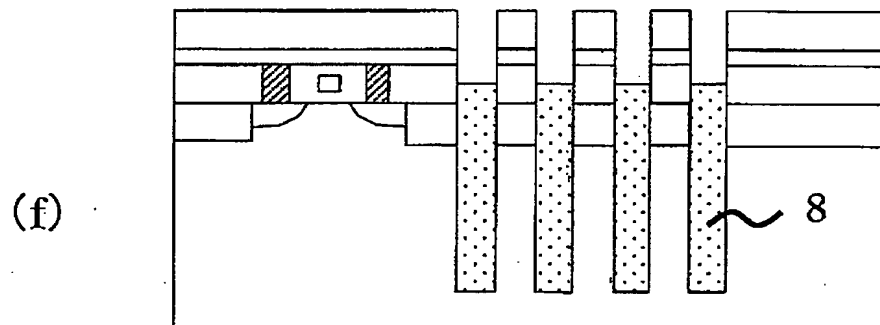
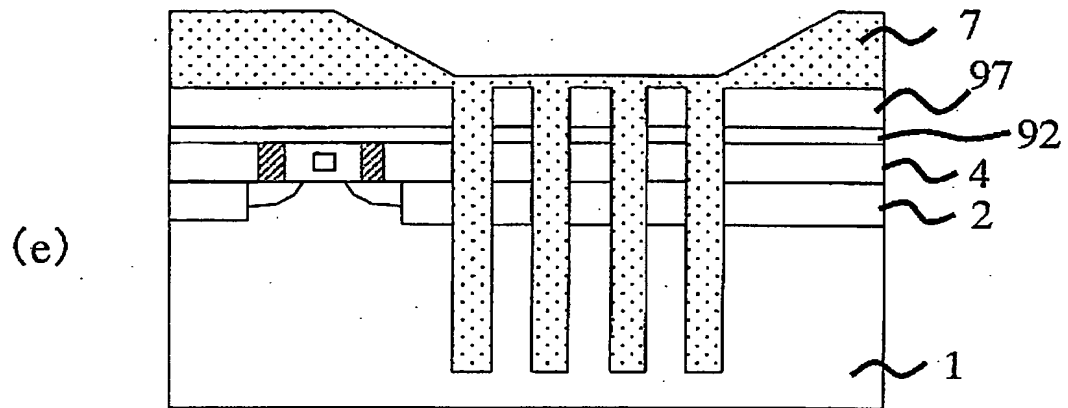
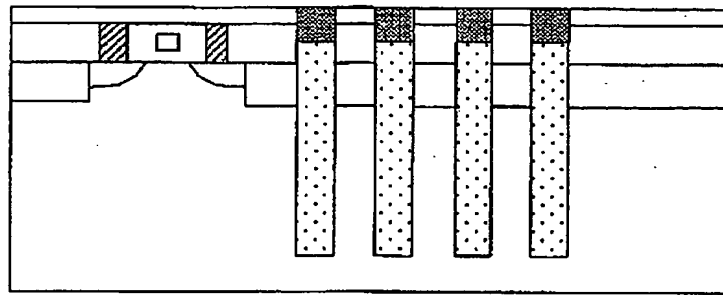
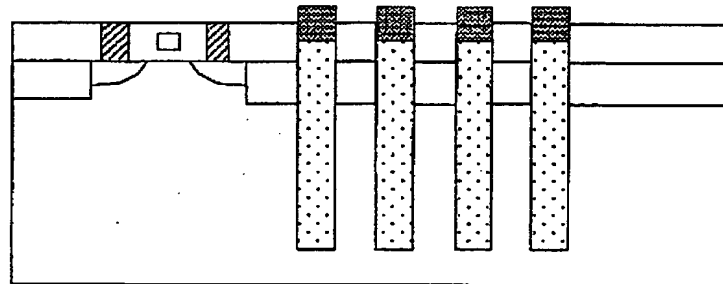


Fig. 50

(h)



(i)



(i)'

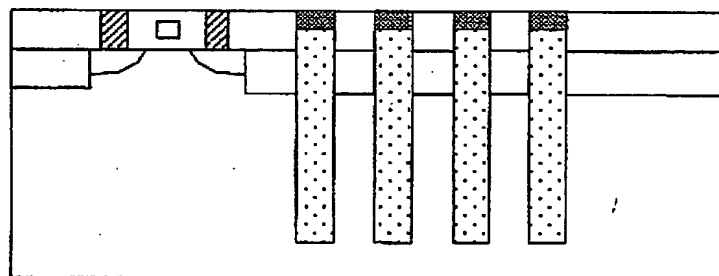


Fig. 51

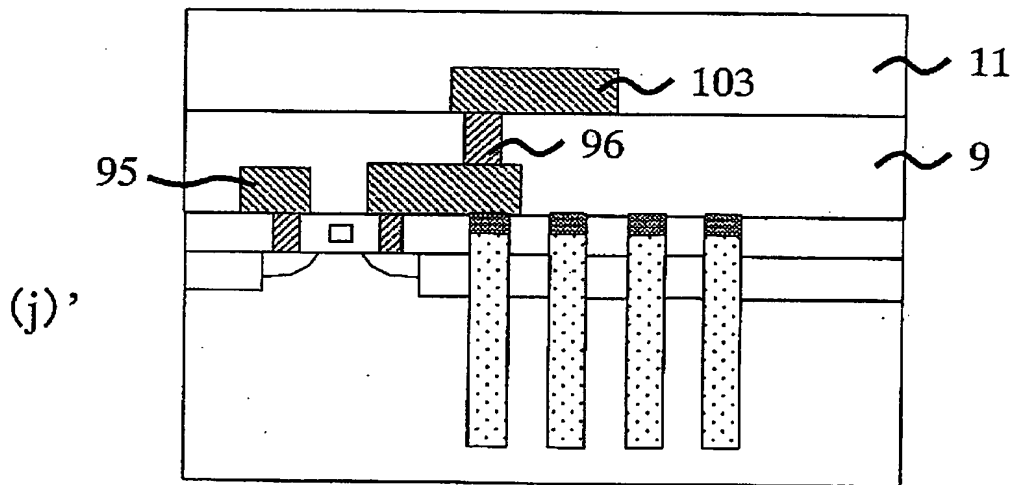
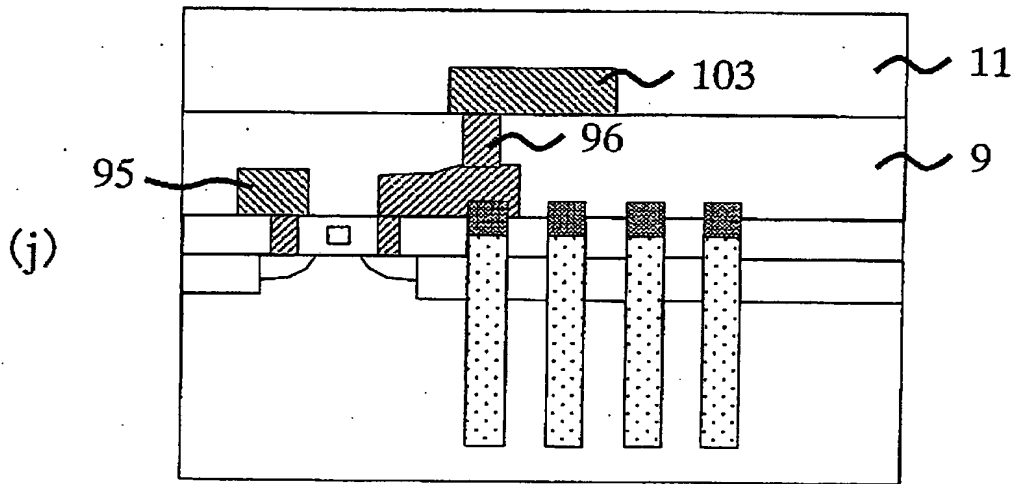


Fig. 52

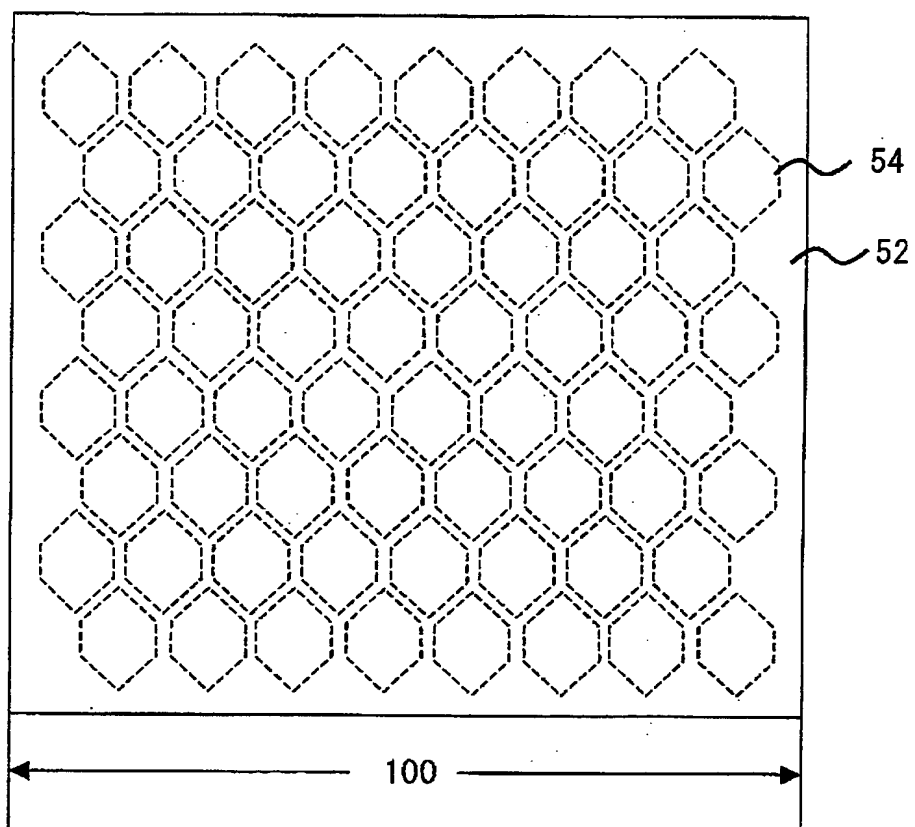


Fig. 53

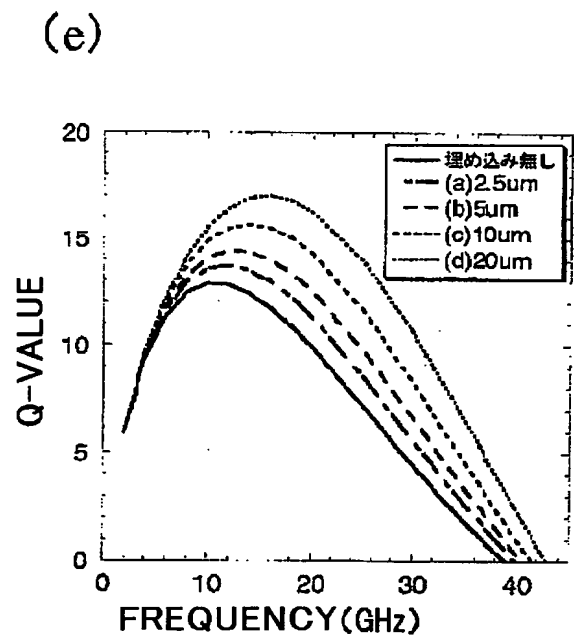
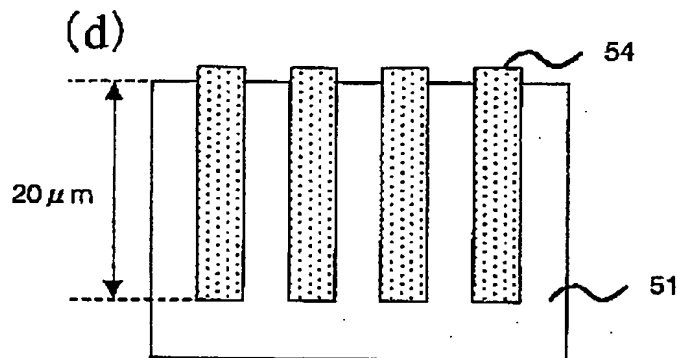
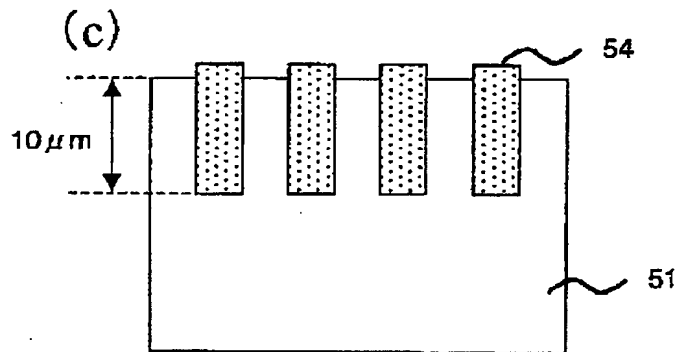
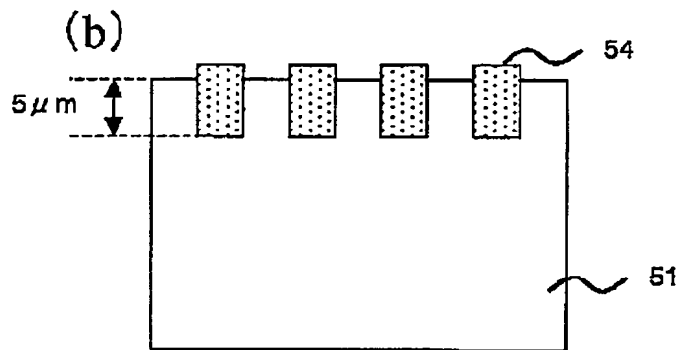
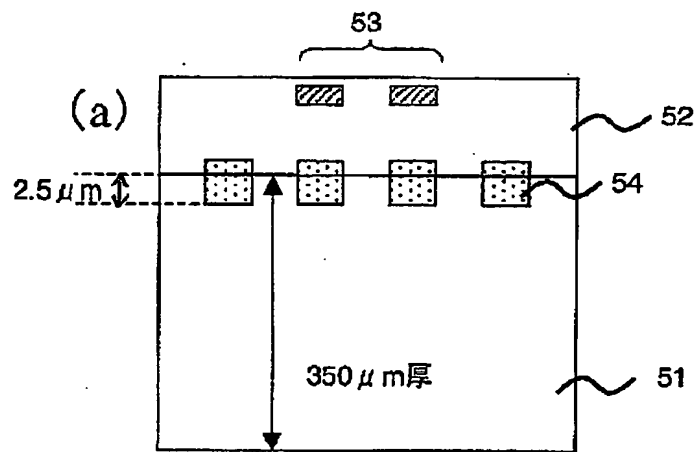
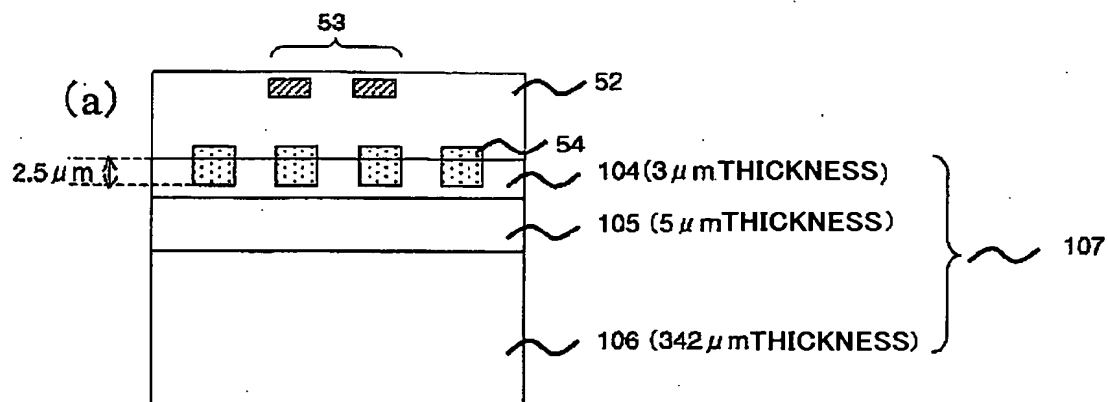


Fig. 54



104 HIGH-RESISTANCE EPITAXIAL LAYER  
 105 LOW-RESISTANCE EPITAXIAL LAYER  
 106 HIGH-RESISTANCE SUPPORT SUBSTRATE  
 107 SEMICONDUCTOR SUBSTRATE INCLUDING  
 A PLURALITY OF LAYERS

